TSEV81102G0FS Evaluation Board

User Guide

e2v

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Section 1
Introduction

1.1 Description

The TSEV81102G0 DMUX Evaluation Board (EB) is designed to simplify the characterization and the evaluation of the TS81102G0 device (1.5 Gsps DMUX). The DMUX EB enables testing of all the DMUX functions, which are:

- Synchronous and asynchronous reset functions
- Selection of the DMUX ratio (1:4 or 1:8)
- Selection of the number of bits (8 or 10)
- Output data common mode and swing adjustment
- Die junction temperature measurements over military temperature range

The DMUX EB is designed to enable easy connection to e2v's ADC Evaluation Boards (for example, TSEV8388BGL and TSEV83102G0BGL) for an extended functionality evaluation (ADC and DMUX multi-channel applications).

The DMUX EB is delivered fully assembled and tested, with a TS81102G0 device implemented on-board and a heat sink assembled on the device.

1.2 Features

- 50Ω input clock and data (differential ECL) through 2.54 mm pitch connectors
- 50Ω demultiplexed output (single-ended ECL) on up to 8 x 2.54 mm pitch connectors
- DMUX functions adjusted by jumpers and potentiometers
- Separated ground and supply planes
- Suitable for high-frequency evaluation of the TS81102G0FS device (up to 1.5 GHz)
- Board dimensions are 200 mm x 190 mm
- Fully assembled and tested

For optimal understanding and use of this evaluation board, please refer to the "TS81102G0FS DMUX" summary specification.

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Section 2
Hardware Description

2.1 Evaluation Board Block Diagram

The evaluation board of the TS81102G0FS DMUX in a CQFP 196 package has been designed with respect to the TSEV81102G0TPZR3 DMUX evaluation board (in the TBGA 240 package).

The same board dimensions and same structure have been used.

There is, however, one main difference between the two boards, which is that the top layer of the TSEV81102G0FS is symmetrical to the one for the TSEV81102G0TPZR3 board. The DMUX in a CQFP 196 package is, in fact, a cavity-up device, while the DMUX in TBGA 240 is a cavity-down device. Consequently, all signals on the DMUX in a CQFP package are mirror images of the ones on the DMUX in a TBGA 240 package.

This results in having to flip the DMUX board over to make it compatible with other e2v ADC boards (such as the TSEV8388Bxx or TSEV83102G0BXX ADC evaluation boards).

In addition, e2v considered placing a hole inside the board for thermal management purposes (for the heat sink).

Figure 2-1 illustrates the board's simplified cross section.

Figure 2-1. TSEV81102G0FS Board Simplified Cross-section (Board Mounting for Compatibility with TSEV8388BF/FZA2 ADC Boards)

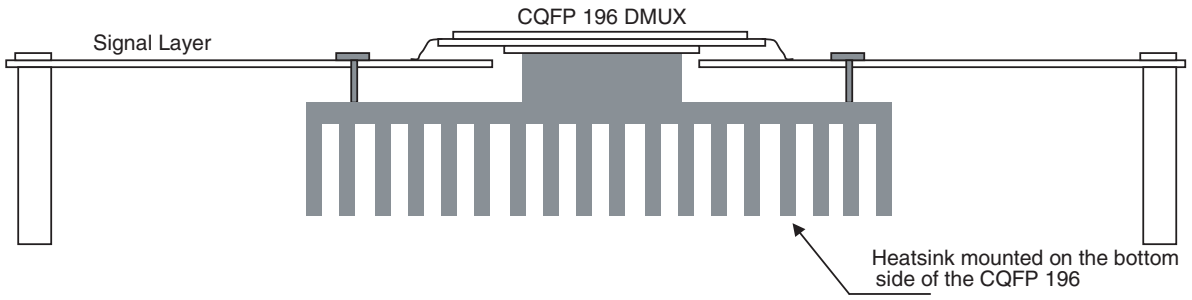


Figure 2-2. TSEV81102G0FS Board to ADC Board Connection (TSEV8388BF/FZA2) Simplified Diagram

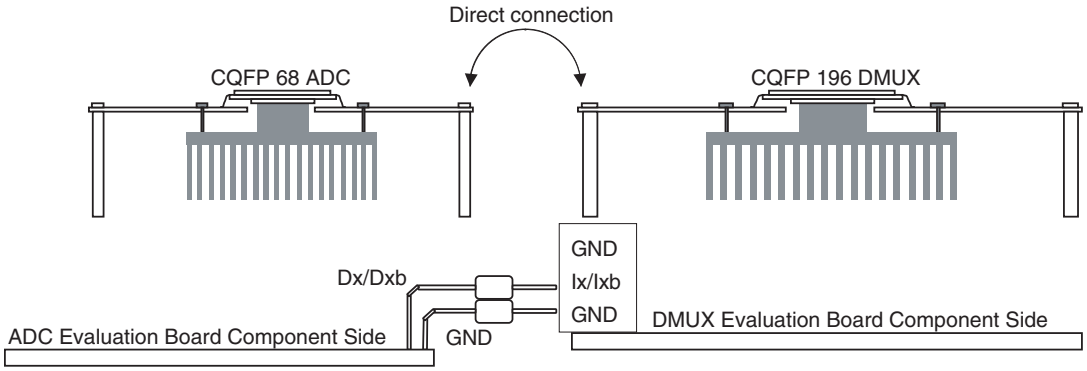


Figure 2-3. TSEV81102G0FS Board Simplified Cross Section (Board Mounting for Compatibility with TSEV8388GL/GLZA2 and TSEV83102G0BGL ADC Boards)

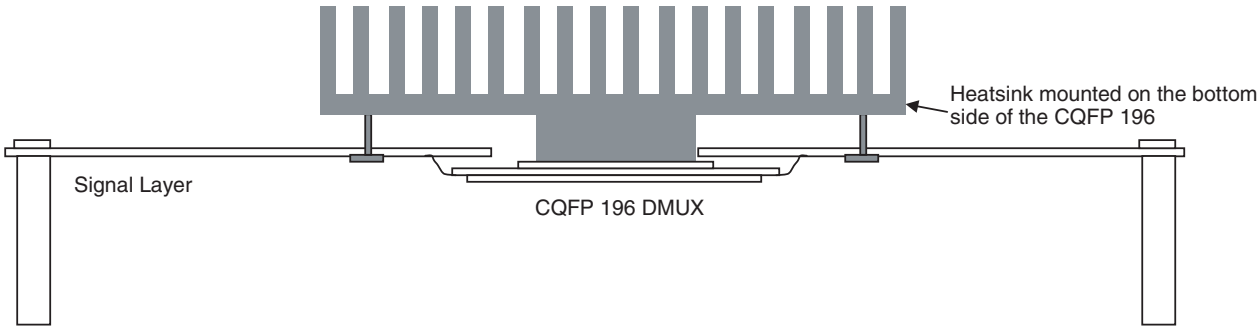


Figure 2-4. TSEV81102G0FS Board to ADC Board Connection (TSEV8388GL/GLZA2 and TSEV83102G0BGL) Simplified Diagram

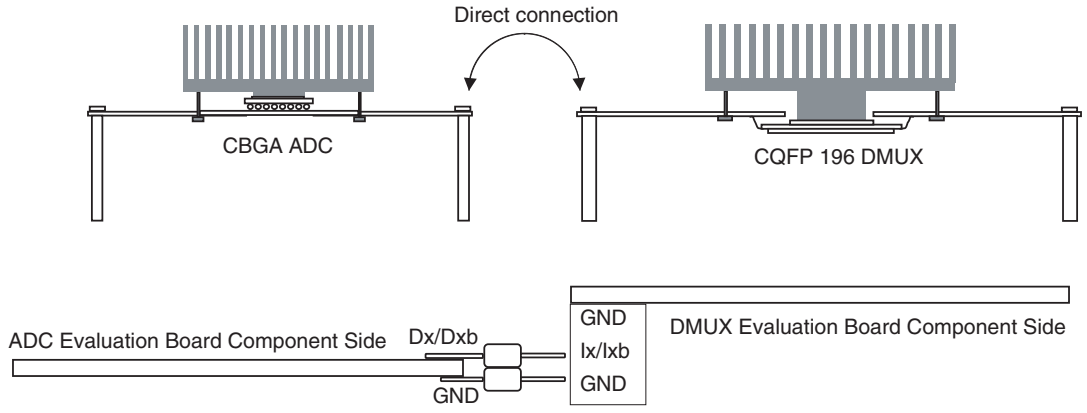
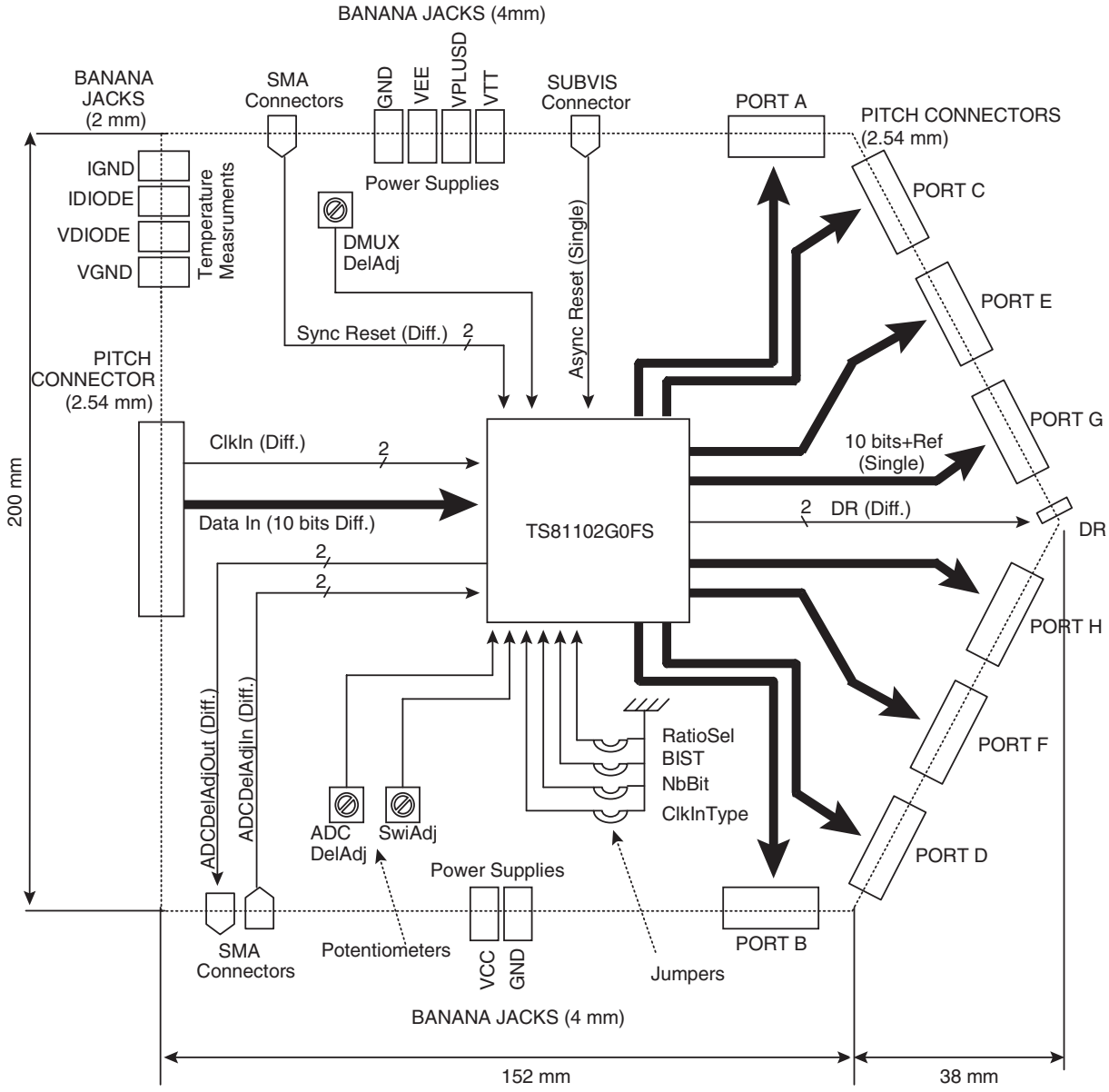


Figure 2-5. TSEV81102G0FS Evaluation Board Block Diagram



2.2 Board Structure

2.2.1 Thickness Profile of Board Layers

The TSEV81102G0 is a seven-layered PCB constituted of four copper layers and three dielectric layers.

The board is 1.6 mm thick. The number of layers, thickness and function of each layer, starting with the top layer, are given in Table 2-1.

Table 2-1. Board Layer Thickness Profiles

Layer	Characteristic
Layer 1 Copper layer	Copper thickness = 35 µm Input signals: 50Ω microstrip lines Output data signals: 60Ω microstrip lines, 50Ω terminated
Layer 2 RO4003 dielectric layer (Hydrocarbon/wovenglass)	Layer thickness = 200 µm Dielectric constant = 3.4 at 10 GHz –0.044 dB/inch loss at 2.5 GHz –0.018 dB/inch loss at 18 GHz
Layer 3 Copper layer	Copper thickness = 35 µm Upper reference plane divided into two parts: GND and V_{PLUSD}
Layer 4 BT/epoxy dielectric layer	Layer thickness = 0.4 mm
Layer 5 Copper layer	Copper thickness = 35 µm Power plane: V_{EE}, V_{CC}, V_{TT}, GND
Layer 6 BT/epoxy dielectric layer	Layer thickness = 860 µm
Layer 7 Copper layer	Copper thickness = 35 µm Lower reference plane

2.2.2 Metal Layers

The four metal layers respectively correspond to:

- The signals' layer (layer 1)
- The two reference layers (layers 3 and 7)
- The supply layer (layer 5)

The upper and lower reference planes (layers 3 and 7) are partitioned into GND (the reference for the input signals) and V_{PLUSD} (the reference for the digital output signals), in the same way as the DMUX package.

The fifth layer is dedicated to power supplies and to ground.

2.2.3 Dielectric Layers

The three dielectric layers are respectively composed of a low insertion loss dielectric (RO4003) layer (layer 2) and BT/epoxy dielectric layers (layers 4 and 6).

Considering the severe mechanical constraints of the wide temperature range and the high frequency domain in which the board is meant to operate, two different dielectric materials are used:

- The first is a low insertion loss RO4003 hydrocarbon/wovenglass dielectric (–0.044 dB/inch loss at 2.5 GHz), which has an enhanced dielectric consistency in the high frequency domain, and is dedicated to the routing of 50Ω and 60Ω traces. The RO4003 dielectric constant is typically 3.4 at 10 GHz.

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- The second is the BT/epoxy layer, chosen for its enhanced mechanical characteristics at elevated temperature operation. The typical dielectric constant is 4.5 at 1 MHz. The BT/epoxy dielectric has enhanced characteristics compared to the FR4 epoxy dielectric, namely:
  - a higher operating temperature value: 170°C (125°C for FR4)
  - better withstanding of thermal shocks (from –65°C up to 170°C)

The characteristics of these two dielectrics make the board particularly suitable for measurements in the high frequency domain and over extended temperature ranges.

2.3 Power Supplies and Ground Access

The power supplies are provided by four 4 mm section red banana jacks for V_{EE}, V_{CC}, V_{TT} and V_{PLUSD} respectively.

The ground access is provided by two 4 mm black banana jacks.

Note: Two distinct GND ground pads have been implemented on the board because of layout considerations. For proper usage, they should be connected together to the same ground.

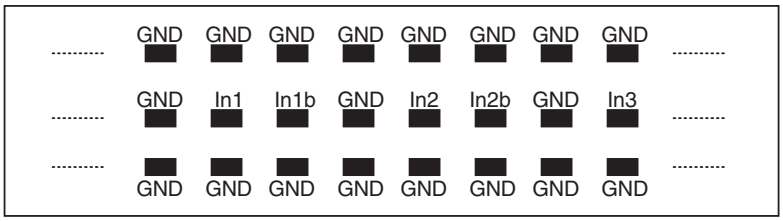
2.4 Input Access

2.4.1 Input Data and Clock Access

Access to the differential data and clock inputs (ClkIn, ClkInb, I[0..9], I[0..9]b) are provided by a 2.54 mm female pitch connector via 50Ω microstrip lines.

The connector is made up of three rows of pitches. The lower row is connected to GND and the upper row is used for the data and clock connections. Each differential signal is separated by a pitch connected to GND, as shown in Figure 2-6.

Figure 2-6. Input Data Pitch Connector



Note: 100Ω differential impedance matching is performed on-chip.

2.4.2 Synchronous Reset Access

Access to the signals *Syncreset* and *Syncresetb* is provided by SMA connectors via 50Ω microstrip lines.

Note: 100Ω differential impedance matching is performed on-chip.

2.4.3 Asynchronous Reset Access

Access to the signal *AsynchReset* is provided by one SMA connector. A push button also allows you to perform a quick asynchronous reset of the board.

2.4.4 ADC Synchronization Input Signal Access

Access to the differential signal *ADCDelAdjIn*/*ADCDelAdjInb* is provided by two SMA connectors via 50Ω microstrip lines.

Note: 100Ω differential impedance matching is performed on-chip.

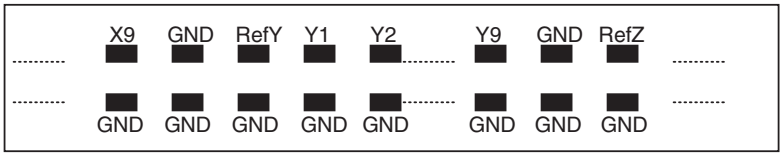
2.5 Output Access

2.5.1 Digital Outputs

Access to the single-ended output data and to the differential output clock (A[0..9] to H[0..9], RefA to RefH, DR, DRb) is provided by male 2.54 mm pitch connectors, via 60Ω microstrip lines. The microstrip lines are 50Ω terminated.

The connectors are made up of two rows of pitches. The upper row is used for the signal connections. The lower row is connected to GND. The output ports are separated from one another by a column (two pitches) connected to GND, as shown:

Figure 2-7. Output Data Pitch Connector



Note: The characteristic impedance of the data output microstrip lines is 60Ω so as to terminate the lines by either 50Ω (ECL, PECL output format) or 75Ω (TTL output format, available on request only).

2.5.2 ADC Synchronization Output Signal Access

Access to the differential signal *ADCDelAdjOut*/*ADCDelAdjOutb* is provided by two SMA connectors, via 50Ω microstrip lines.

2.6 DMUX Function Settings

Four 2 mm section banana jacks are provided to perform die temperature measurements (see Section 5.3).

Three potentiometers are provided for the adjustment of *SWIADJ*, *ADCDelAdCtrl* and *DMUXDelAdjCtrl* respectively.

Four jumpers are provided for the settings of the static control signals *NBBIT*, *RATIOSEL*, *CLKINTYPE* and *BIST* (jumper on = logic '0', jumper off = logic '1').

2.7 Layout Information

The DMUX processes high-frequency signals and as such particular attention was given to the board's layout to achieve full-speed operation efficiency. The length of the transmission lines for both the input and output signals have been matched. In addition, cross-talk effects for the output data have been reduced by increasing, wherever possible, the space between the lines.

Note: It is recommended to route the input data with differential lines whenever possible.

2.7.1 Decoupling of Power Supplies

Each power supply is decoupled by a 1 µF tantalum capacitor in parallel to a 100 nF chip capacitor.

Each power supply access of the DMUX is bypassed as close as possible to the device by 10 nF and 100 pF surface mount chip capacitors side by side.

Note: These capacitors are superimposed with the capacitor of lowest value soldered first.

2.7.2 Reference Planes

Each reference plane (layers 3 and 7) is physically divided into two parts: one GND plane and one V_{PLUSD} plane, which is the voltage reference for the output buffers of the

DMUX. V_{PLUSD} can be set to all levels between GND and 3.3V, allowing the DMUX to be set in various output modes (ECL with V_{PLUSD} = GND, PECL with V_{PLUSD} = 3.3V, etc.).

2.7.3 I/O Transmission Lines

Table 2-2 summarizes the main properties of the microstrip lines of all the input and output signals.

Note: The transmission delay through a transmission line is approximately 6.1 ps/inch.

Table 2-2. I/O Transmission Lines

Signal	Type	Typical length	Length Matching	Characteristic impedance	Adaptation	Comments
ClkInClkInb	Differential	68.2 mm 68.2 mm	--	50Ω	On-chip 100Ω differential	
I[0..9], I[0..9]b	Differential	68.9 mm	±1	50Ω	On-chip 100Ω differential	Min. length (I1B): 68.3 mm Max length (I0B): 69.6 mm
A[0..9], …, H[0..9]	Single-ended	120 mm	±8	60Ω	50Ω	Min. length (F3 & E5):112 mm Max length (C9): 127.9 mm
DRDRb	Differential	113.5 mm 113.5 mm	-	60Ω	50Ω	
SyncResetSyncResetb	Differential	85.7 mm	±1	50Ω	On-chip 100Ω differential	
ADCDelAdjInADCDelAdjInb	Differential	100 mm	±1	50Ω	On-chip 100Ω differential	
ADCDelAdjOut ADCDelAdjOutb	Differential	106 mm	±1	50Ω	None	

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Section 3

Operating Characteristics

3.1 Output Characteristics

In this section, the typical values of the board's I/O signals and power sources are listed. These values refer to a nominal use of the evaluation board, they are purely indicative and may depend on temperature, frequency of use and other parameters.

The following table gives three examples for the DMUX output level settings: ECL, PECL and TTL.

Note: One can set the DMUX to several other output formats as long as the buffer output current remains below 36 mA and V_{PLUSD} stays below 4V with V_{PLUSD} - V_{EE} < 8.3V. The output levels are thus given by the following equations:

$$Voh = \left(\frac{\beta R}{\beta R + 600}\right)\left(V_{PLUSD} - Vbe + \frac{600}{\beta R} Vtt\right)$$

$$Vol = \left(\frac{\beta R}{\beta R + 600}\right)\left(V_{PLUSD} - Vbe - \frac{600}{480}(Vrefsa - VEE - Vbe) + \frac{600}{\beta R} Vtt\right)$$

$$Vref = \left(\frac{\beta R}{\beta R + 600}\right)\left(V_{PLUSD} - Vbe - \frac{600}{960}(Vrefsa - VEE - Vbe) + \frac{600 \times Vtt}{\beta R}\right)$$

Note: β = 100 and Vbe = 0.9V at ambient temperature and 0.6V at high temperature.

Table 3-1. Examples of Output Buffer Format Settings

Parameter	ECL	PECL	TTL	Unit
V_{PLUSD}	0	3.3	3.3	V
V_{TT}	–2	1.3	0	V
Swing	±0.5	±0.5	±1	V
Reference	–1.58	1.72	1.28	V
V_{OH}	–1.02	2.28	2.28	V
V_{OL}	–1.99	1.31	0.28	V
Load	50	50	>75	W
Average output current	14	14	15	mA

3.2 Electrical Characteristics

Table 3-2 lists the board's absolute maximum ratings.

Table 3-2. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6	V
Positive output buffer supply voltage	V_{PLUSD}		GND to 4	V
Negative supply voltage	V_{EE}		GND to –4	V
Analog input voltages	ADCDelAdjCtrl ADCDelAdjCtrlb DMUXDelAdjCtrl DMUXDelAdjCtrlb SwiAdj	Voltage range for each pad Differential voltage range	–1 to 1	V
ECL 50Ω input voltage	ClkIn; ClkInbI[0…9] I[0…9]bSyncReset SyncResetbADCDelAdjIn ADCDelAdjInb	Voltage range for each pad	–2.2 to 0.6	V
Maximum difference between ECL 50Ω input voltages	ClkIn; ClkInbI [0…9]; I[0…9]b SyncReset, Syncresetb ADCDelAdjIn ADCDelAdjInb	Minimum differential swing Maximum differential swing	0.1 2	V
Data output current	A[0…9] to H[0…9] RefA to RefH DR, DRb	Maximum current	36	mA
TTL input voltages	ClkIn Type RatioSel NbBit AsyncReset BIST		GND to V_{CC}	V
Maximum input voltage on diode for temperature measurement	DIODE		700	mV
Maximum input current on diode	DIODE		8	mA
Maximum junction temperature	T_J		135	°C
Storage temperature	Tstg		–65 to 150	°C

Note: Absolute maximum ratings are limiting values, to be applied individualy, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device long-term reliability.

Table 3-3. Recommended Operating Conditions

Parameter	Symbol	Comments	Min.	Typ.	Max.	Unit
Positive supply voltage	V_{CC}		4.75	5	5.25	V
Positive output buffer supply voltage	V_{PLUSD}	ECL output compatibility	0	0	0	V
		PECL output compatibility	3.13	3.3	3.46	V
		TTL output compatibility		3.3		V
Negative supply voltage	V_{EE}		–5.25	–5	–4.75	V
Operating junction temperature	T_J	Commercial grade “C” Industrial grade “V” Military grade “M”	$0 < T_C; T_J < 90$ $–40 < T_C; T_J < 110$ $–55 < T_C; T_J < 125$			°C

3.3 Operating Characteristics

Please refer to the “TS81102G0FS DMUX” specification.

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Section 4

Application Information

4.1 Introduction

Please refer to the “TS81102G0FS” device datasheet for more information on the DMUX functions.

4.2 Quick Start

The evaluation board is delivered fully assembled and tested. A heat sink, which is mandatory to keep the device within the recommended junction temperature conditions, is also delivered and assembled on-board.

Caution: The board’s power supplies must not be turned on until all power connections to the evaluation board are established.

The aim of the following procedure is to help you start the board for the first time.

It describes the step-by-step process you must follow to accomplish a BIST sequence (Built-In Self Test, see Section 4.4) in order to verify if the board is functional.

At the end of the procedure, the DMUX will be configured with these settings:

- DR mode
- 10-bit mode
- 1:8 ratio
- BIST active
- SWIADJ = 0V
- ECL output format

4.2.1 Procedure

1. Connect the board's ground accesses together.
2. Connect V_{PLUSD} to GND (to set the DMUX in ECL output format).
3. Connect a –5V power supply source to $V_{EE.}$ Then connect the supply's ground to GND.
4. Connect a 5V power supply source to V_{CC}. Then connect the supply's ground to GND.
5. Connect a –2V power supply source to $V_{TT.}$ Then connect the supply's ground to GND.
6. Connect a signal generator to the DMUX CLKIN and CLKINB clock input pitches. The DMUX input clock can be either differential or single-ended.

7. Remove the jumpers labeled NBBIT and CLKINTYPE (in order to set the DMUX in 10-bit DR mode.) The remaining jumpers are RATIOSEL (1:8 ratio) and BIST (BIST active).
8. Connect a high-speed logic analyzer to the board's output connector. We recommend that at least one DMUX output port be fully probed.
9. Turn on the supply and signal sources in the following order:
   – V_{EE} first
   – V_{CC}
   – V_{PLUSD}
   – V_{TT}
   – Input clock
10. Set the potentiometer labeled SWIADJ so that the SWIADJ pin of the DMUX is at 0V.
11. Apply the ASYNCRESET by pressing the corresponding button to start the DMUX (the ASYNCRESET signal is active at high TTL level).

At the output, the demultiplexed BIST sequence should be observed (see Section 4.4).

4.3 Adjustments to DMUX Setting

Four jumpers are provided to activate the RATIOSEL, BIST, CLKINTYPE and NBBIT functions. When the jumper is on-board it corresponds to logic "0". The following table gives the DMUX settings for the RATIOSEL, NBBIT, BIST and CLKINTYPE jumper positions.

Table 4-1. DMUX Setting Adjustments

Name	Jumper	Function
CLKINTYPE	ON	DR/2 mode
	OUT	DR mode
BIST	ON	BIST active
	OUT	BIST inactive
NBBIT	ON	8-bit mode
	OUT	10-bit mode
RATIOSEL	ON	1:8 ratio
	OUT	1:4 ratio

4.4 BIST

The bist sequence is a 10-bit 512-code pseudo-random sequence defined by the following equation:

$$N(i)= \left[2 \times N(i-1) + \left[\left[int\left(\frac{N(i-1)}{256}\right) \%2\right] + \left[int\left(\frac{N(i-1)}{16}\right) \%2\right]\right] \%2\right] \%1024$$

with N(0) = 2 and i_0 = 1

The sequence starts on port A. The driving clock during the BIST sequence is CLKIN.

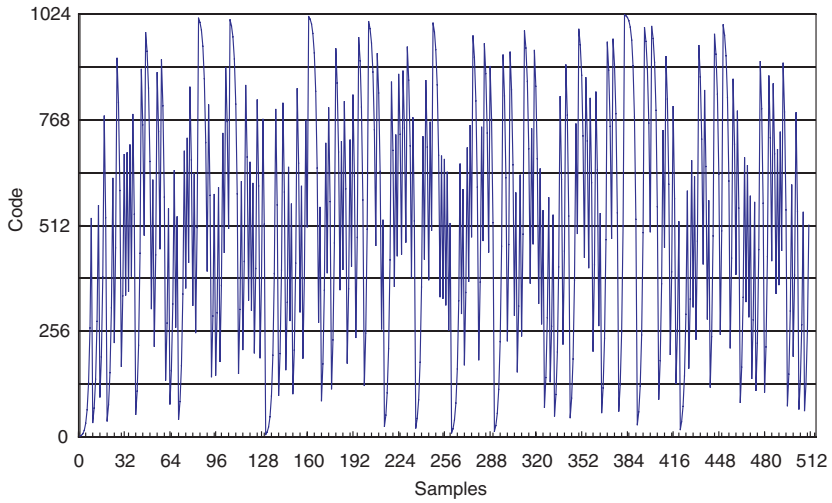
Depending on the selected ratio, the BIST can be seen on ports A to H (1:8 ratio) or on ports A to D (1:4 ratio).

Since the BIST is a 10-bit sequence, we recommend setting the NBBIT signal to logic “1” for 10-bit mode (jumper out).

CLKINTYPE must be set to logic “1” (jumper out).

The following figure shows the BIST sequence.

Figure 4-1. BIST Sequence



Note: The complete BIST sequence is available on request.

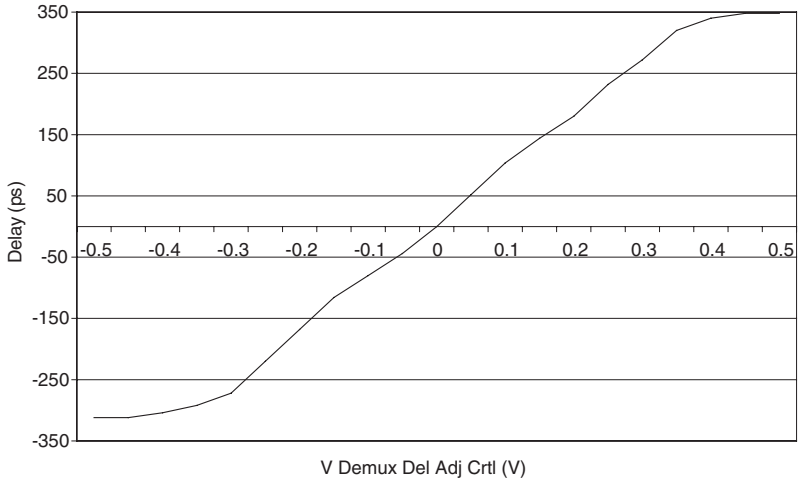
4.5 Delay Adjust Function

Two delay adjusts of ±250 ps controlled by potentiometers are available to synchronize the input clock and the DMUX data on the one hand, and delay the signal *ADCDelAdjIn* on the other.

- The input signal *DelAdjCtrl* is tied to GND.
- The input signal *DelAdjCtrlb* can vary from -0.55V to 0.55V, depending on the potentiometer position.
- The generated delay is proportional to the differential across *DelAdjCtrl* and

DelAdjCtrlb, as shown in Figure 4-2 on page 4.

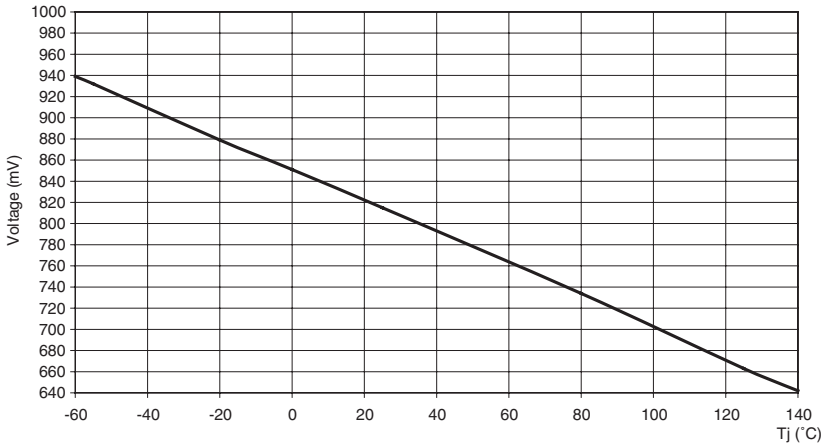
Figure 4-2. Delay Adjustment Characteristics (T_J = 60°C)



Note: The variation of the delay depending on the temperature is insignificant.

4.6 Die Junction Temperature Monitoring

Figure 4-3. Diode for Die Junction Temperature Monitoring Characteristics (I = 1 mA)



4.7 Applying the TSEV81102G0FS DMUX to e2v ADC Evaluation Boards

The TSEV81102G0FS DMUX evaluation board is designed to be fully compatible with e2v's TSEV8388B and TSEV83102G0B ADC evaluation boards.

Figure 4-4 on page 5 shows the ADC and DMUX board connections and Table 4-2 provides the required configuration to match the DMUX board with the ADC board.

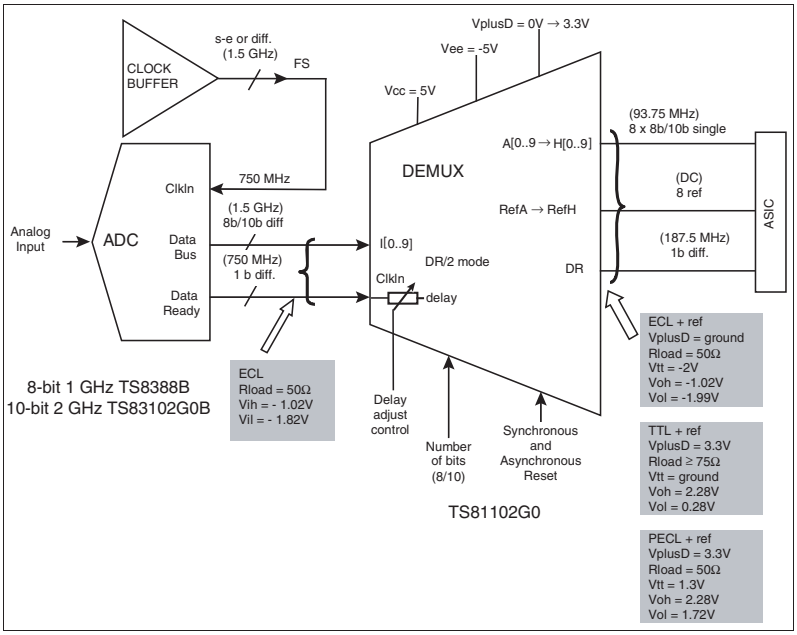
When used with the TSEV8388BF/FZA2 boards, the TSEV81102G0FS DMUX board can be plugged directly to the ADC output connector with the DMUX device on top of the board.

When it is used with the TSEV8388BGL/GLZA2 or TSEV83102G0BGL ADC boards, the TSEV81102G0FS DMUX board must be turned over, with the device on the bottom of the board and I0 matched with D0 of the ADC board.

Table 4-2. ADC and DMUX Board Connections

TSEV8388BF/FZA2	TSEV81102G0FS (Device on Top)	TSEV8388BGL/GLZA2 or TSEV83102G0BGL	TSEV81102G0FS (Device at the Bottom)
D0	I0	D0	I0
D1	I1	D1	I1
D2	I2	D2	I2
D3	I3	D3	I3
D4	I4	D4	I4
D5	I5	D5	I5
D6	I6	D6	I6
D7	I7	D7	I7
-	I8 not connected	(D8)	I8 (if applicable)
-	I9 not connected	(D9)	I9 (if applicable)

Figure 4-4. ADC and DMUX Evaluation Board Interfaces



4.8 Miscellaneous

For proper usage of the board, we recommend the following:

- Always wear an anti-static strap when manipulating the board as the DMUX is very sensitive to electrostatic discharge (ESD).
- Make sure the current delivered by the power supply is sufficient to supply the board.
- Always switch on the DMUX board supplies in the following order: V_{EE} first, V_{CC}, V_{PLUSD} and VTT.

- Always make sure the output current through the termination resistors does not exceed 36 mA.
- After the supplies are switched on, send an asynchronous reset pulse into the DMUX (i.e. leave the pad ASYNCRESET open and then connect it to ground) in order to start the device.

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Section 5

Package Description

5.1 Pin Description

Table 5-1. Pin Description

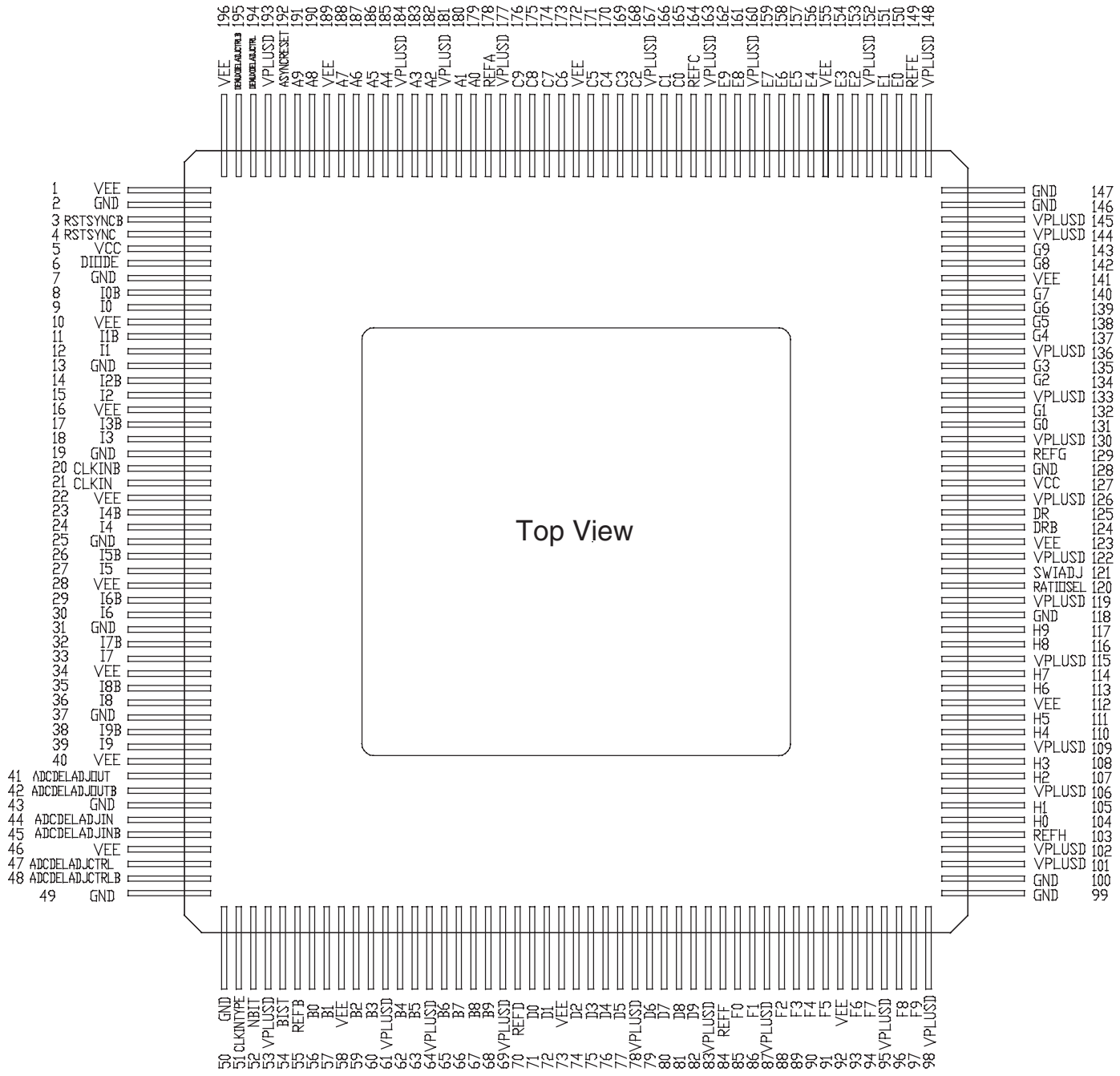
Symbol	Pin Number	Description
Power Supplies		
V_{CC}	5, 127	Positive 5V power supply
V_{EE}	1, 10, 16, 22, 28, 34, 40, 46, 58, 73, 92, 112, 123, 141, 155, 172, 189, 196	Negative -5V power supply
V_{PLUSD}	53, 61, 64, 69, 78, 83, 87, 95, 98, 101, 102, 106, 109, 115, 122, 126, 130, 133, 136, 144, 145, 148, 152, 160, 163, 167, 177, 181, 184, 193	Output buffer power supply
GND	2, 7, 13, 19, 25, 31, 37, 43, 49, 50, 99, 100, 118, 128, 146, 147	Ground
Analog Input Signals		
DMUXDelAdjCtrl	194	In-phase DMUX clock delay cell control signal
DMUXDelAdjCtrlB	195	Inverted phase DMUX clock delay cell control signal
ADCDelAdjCtrl	47	In-phase stand-alone delay cell control signal
ADCDelAdjCtrlB	48	Inverted phase stand-alone delay cell control signal
SwiAdj	121	Swing adjust function control signal
DIODE	6	Die junction temperature monitoring signal
ECL Input Signals		
ClkIn	21	In-phase input clock signal
ClkInB	20	Inverted phase input clock signal
I[0…9]	9, 12, 15, 18, 24, 27, 30, 33, 36, 39	In-phase input data
I[0…9]B	8, 11, 14, 17, 23, 26, 29, 32, 35, 38	Inverted phase input data
SyncReset	4	In-phase synchronous reset
SyncResetB	3	Inverted phase synchronous reset

Table 5-1. Pin Description (Continued)

Symbol	Pin Number	Description
ADCDelAdjIn	44	In-phase input of the stand-alone delay cell
ADCDelAdjInB	45	Inverted phase input of the stand-alone delay cell
Output Data		
A[0…9]B[0…9]C[0…9] D[0…9]E[0…9]F[0…9] G[0…9]H[0…9]	179, 180, 182, 183, 185, 186, 187, 188, 190, 191, 56, 57, 59, 60, 62, 63, 65, 66, 67, 68, 165, 166, 168, 169, 170, 171, 173, 174, 175, 176, 71, 72, 74, 75, 76, 77, 79, 80, 81, 82, 150, 151, 153, 154, 156, 157, 158, 159, 161, 162, 85, 86, 88, 89, 90, 91, 93, 94, 96, 97, 131, 132, 134, 135, 137, 138, 139, 140, 142, 143, 104, 105, 107, 108, 110, 111, 113, 114, 116, 117	Output data
RefA to RefH	178, 55, 164, 70, 149, 84, 129, 103	Reference outputs (tied to the common mode voltage of each port)
DR	125	In phase data ready signal (centered on the output data, frequency = output data/2)
DRB	124	Inverted phase data ready signal (centered on the output data, frequency = output data/2)
TTL Input Signals		
ClkInType	51	Input clock type: - DR mode = logic “1” - DR mode = logic “0”
RatioSel	120	DMUX ratio selection: - 1:4 mode = logic “0”
NbBit	52	Number of bits selection: - 10 bits = logic “1” - 8 bits = logic “0”
AsyncReset	192	Asynchronous reset (active high)
BIST	54	Built-in self-test mode (active low)
Other Output Signals		
ADCDelAdjOUT	41	In-phase output of the stand-alone delay cell
ADCDelAdjOUTB	42	Inverted phase output of the stand-alone delay cell

5.2 Enhanced CQFP 196 Pinout

Figure 5-1. CQFP 196 Package Pinout



5.3 CQFP 196 Outline Dimensions

- Package: black AI203 ceramic
- Leads: Kovar, Ni and Au plating
- Lid: Kovar, Ni and Au plating
- Heat spreader on the bottom: CuW with Ni and Au plating

Figure 5-2. CQFP 196 Package Top View

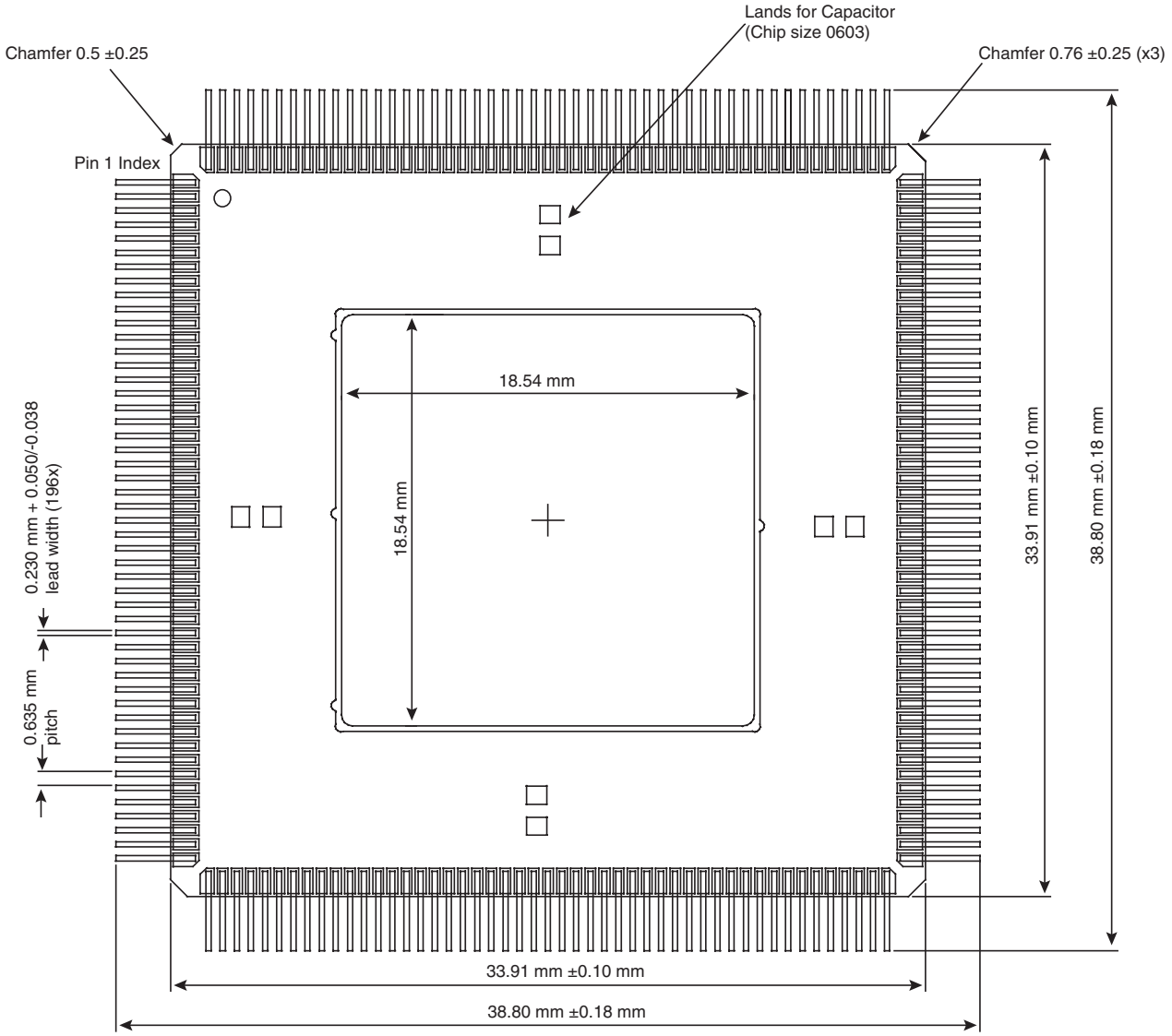


Figure 5-3. CQFP 196 Cross Section - Low Stand-off

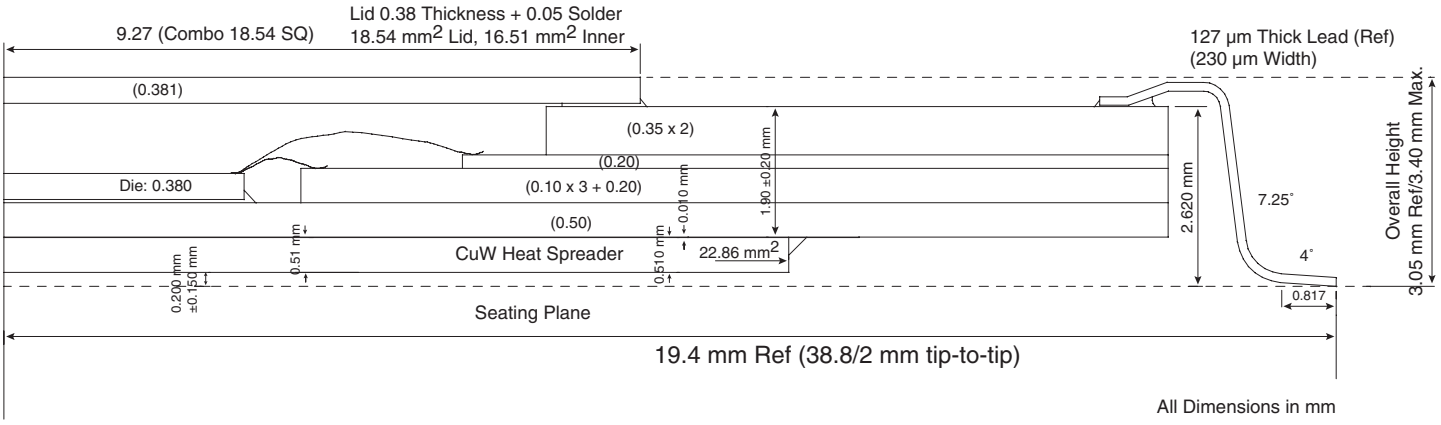
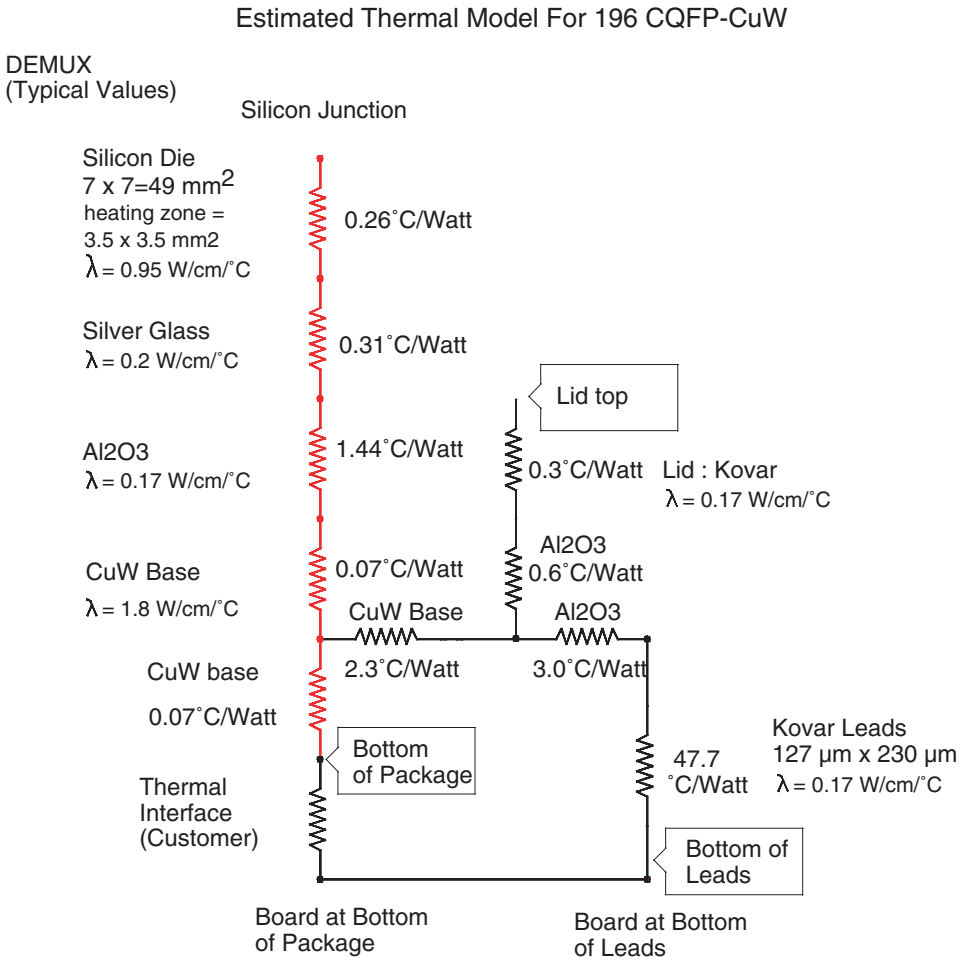


Figure 5-4. Thermal Characteristics



Thermal Resistance Junction to bottom of case =
0.26 + 0.31 + 1.44 + 0.07 + 0.07 = 2.15˚C/Watt
(customer thermal interface excluded)

e2v

Section 6

Ordering Information

6.1 Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
TS81102G0VFS	CQFP 196	“V” grade –40°C < Tc; Tj < 110°C	Standard	Contact e2v sales
TS81102G0MFS	CQFP 196	“M” grade –55°C < Tc; Tj < 125°C	MIL	Contact e2v sales
TS81102G0MFS9NB1	CQFP 196	“M” grade –55°C < Tc; Tj < 125°C	ESA/SCC	Contact e2v sales
TSEV81102G0FS	CQFP 196	Ambient	Prototype	Contact e2v sales

Section 7

Appendices

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7.1 Electrical Schematics

Figure 7-1. TSEV81102G0FS Electrical Schematics

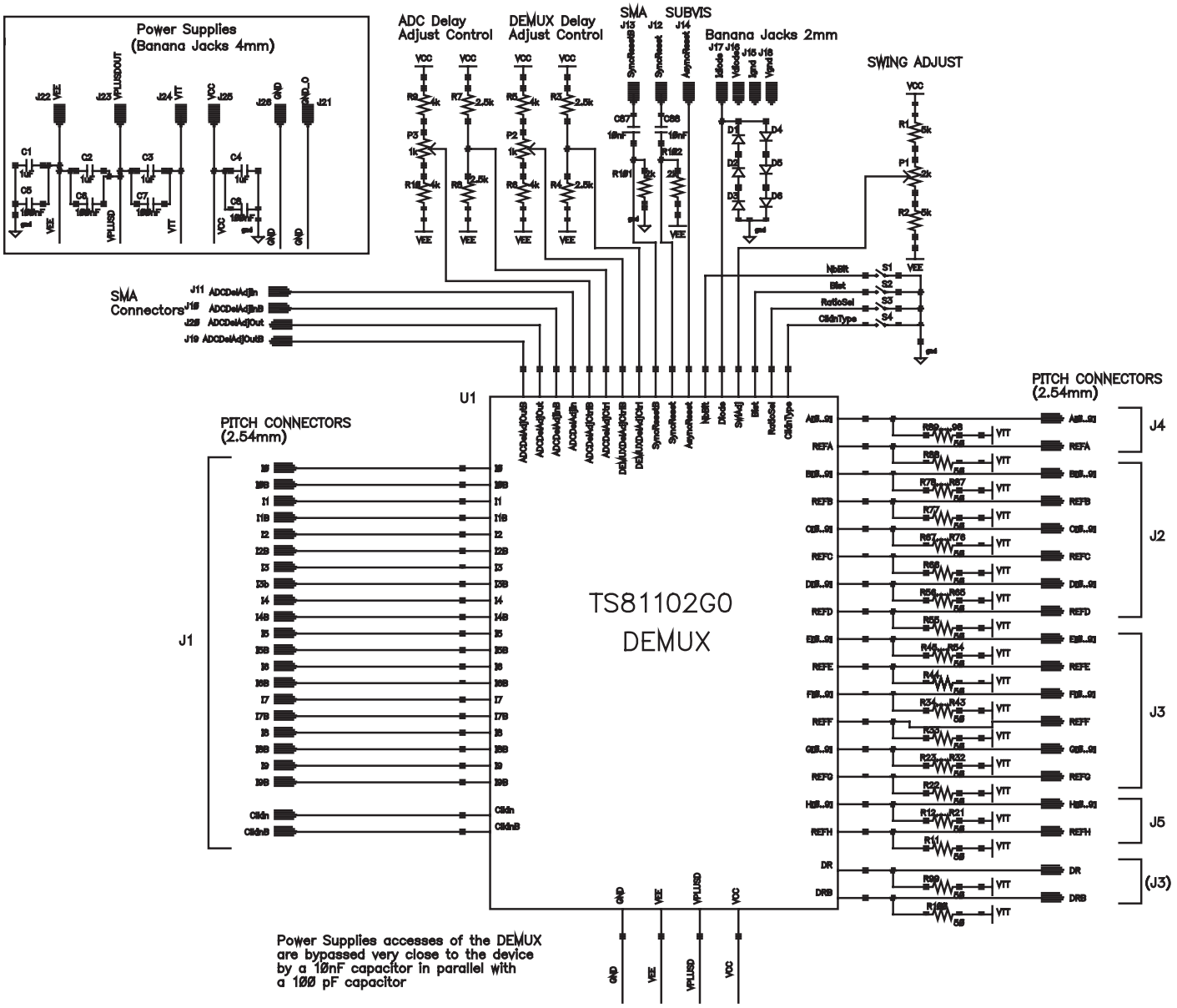

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Figure 7-2. TSEV81102G0FS Component Layer (Top)

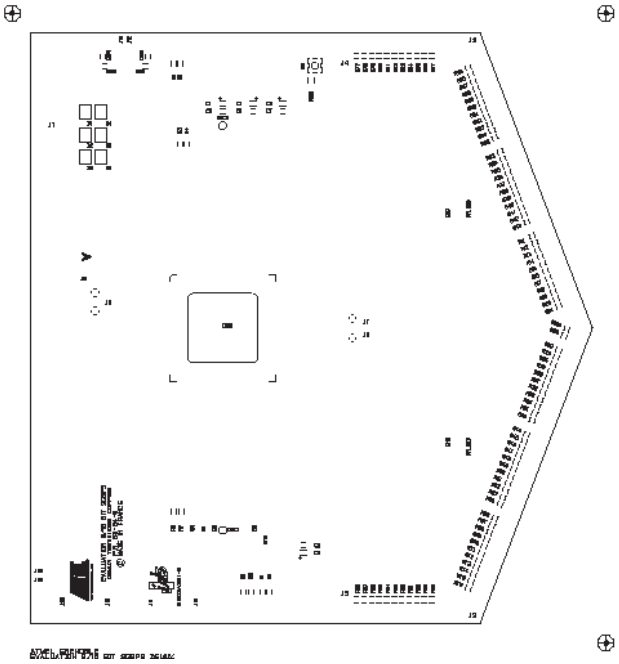

Figure 7-3. TSEV81102G0FS Component Layer (Bottom)

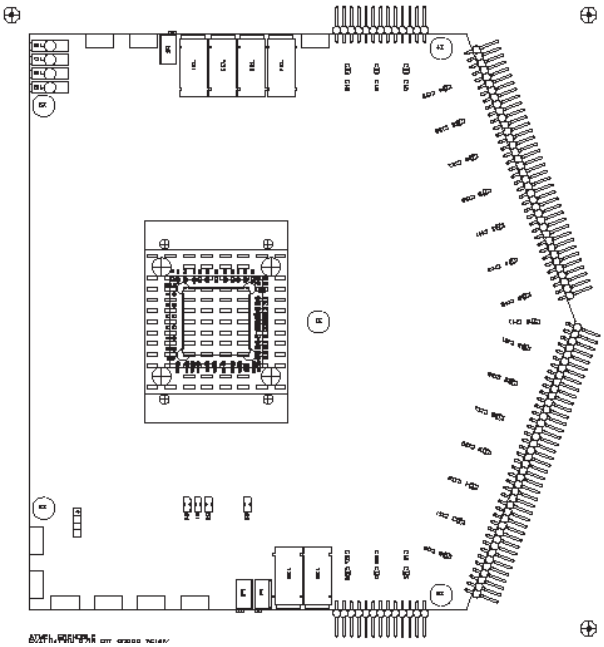

Figure 7-4. TSEV81102G0FS Top Layer

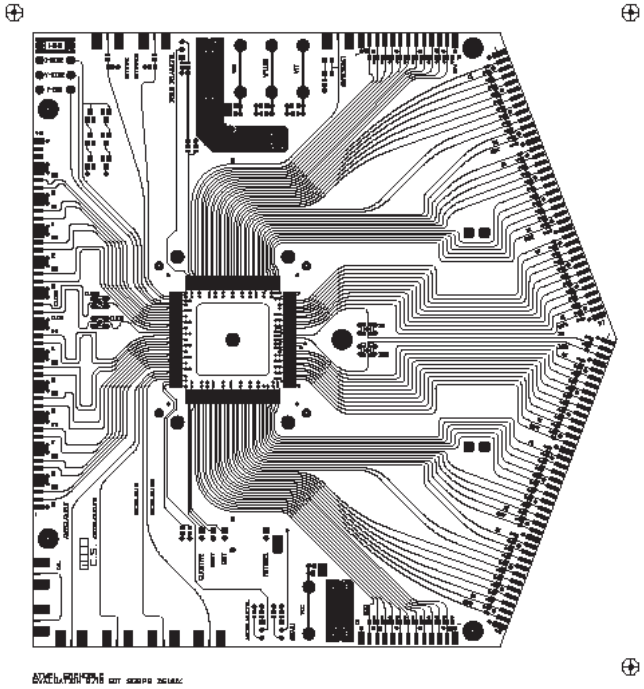

Figure 7-5. TSEV81102G0FS Second Layer (GND and V_{PLUSD})

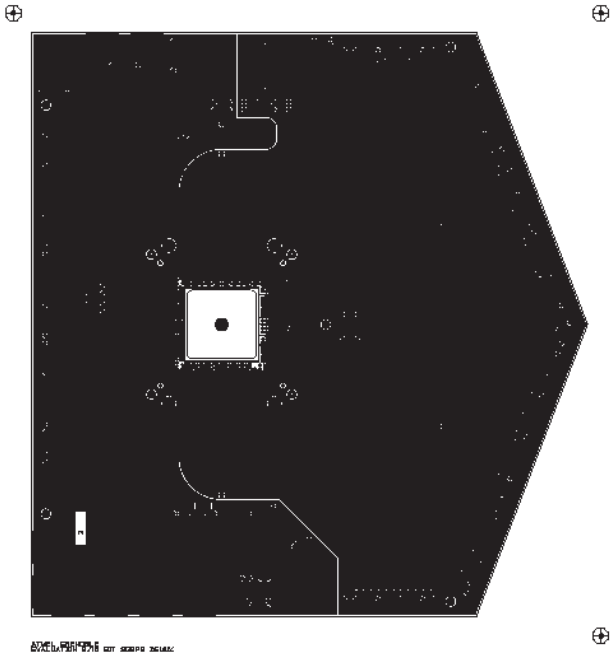

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Figure 7-6. TSEV81102G0FS Third Layer (GND and Power Supplies)

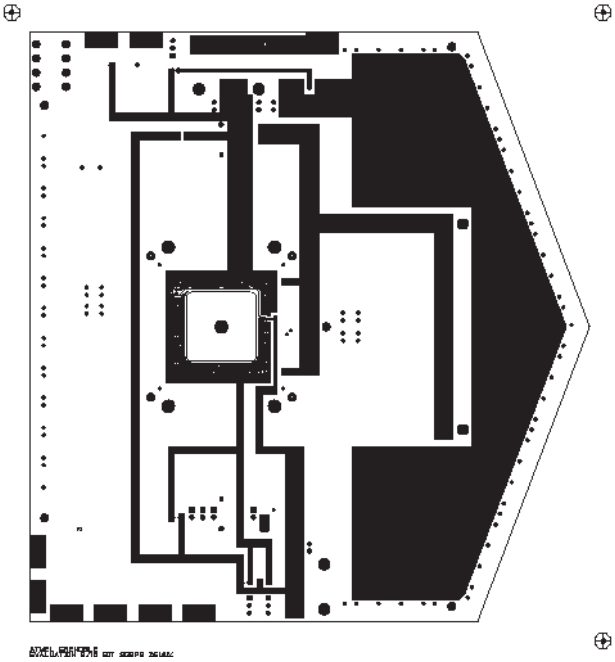
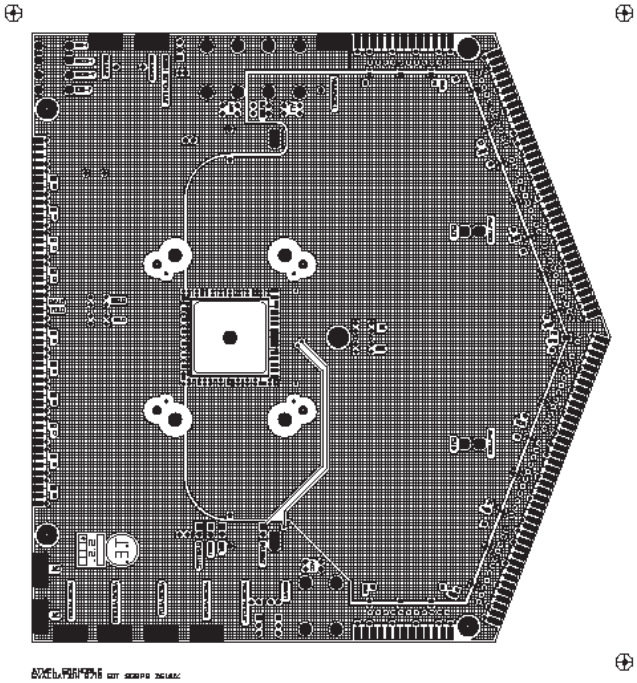


Figure 7-7. TSEV81102G0FS Fourth Layer (GND, V_{PLUSD} and Miscellaneous)



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