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EV12DS130ZPY-EB

User Guide

Table of Contents

e2v

Section 1
Introduction

1.1 Scope

The EV12DS130ZPY-EB evaluation board is designed to facilitate the evaluation and characterization of the EV12DS130 12-bit DAC with 4/2:1 MUX in fpBGA package.

The EV12DS130ZPY-EB Evaluation Kit includes:

- One MUXDAC evaluation board
- A cable for connection to the RS-232 port
- One CD-ROM that contains the software Tools necessary to use the SPI

The evaluation system of the EV12DS130 MUXDAC device consists in a configurable printed circuit board, including the soldered MUXDAC device, an FPGA chip, a serial interface and a user interface running on that platform.

1.2 Description

The EV12DS130ZPY evaluation board is very straightforward as it implements e2v EV12DS130 12-bit MUXDAC device, ALTERA FPGA STRATIX II EP2S60F672C5N, SMA connectors for the sampling clock, analog outputs and reset inputs accesses.

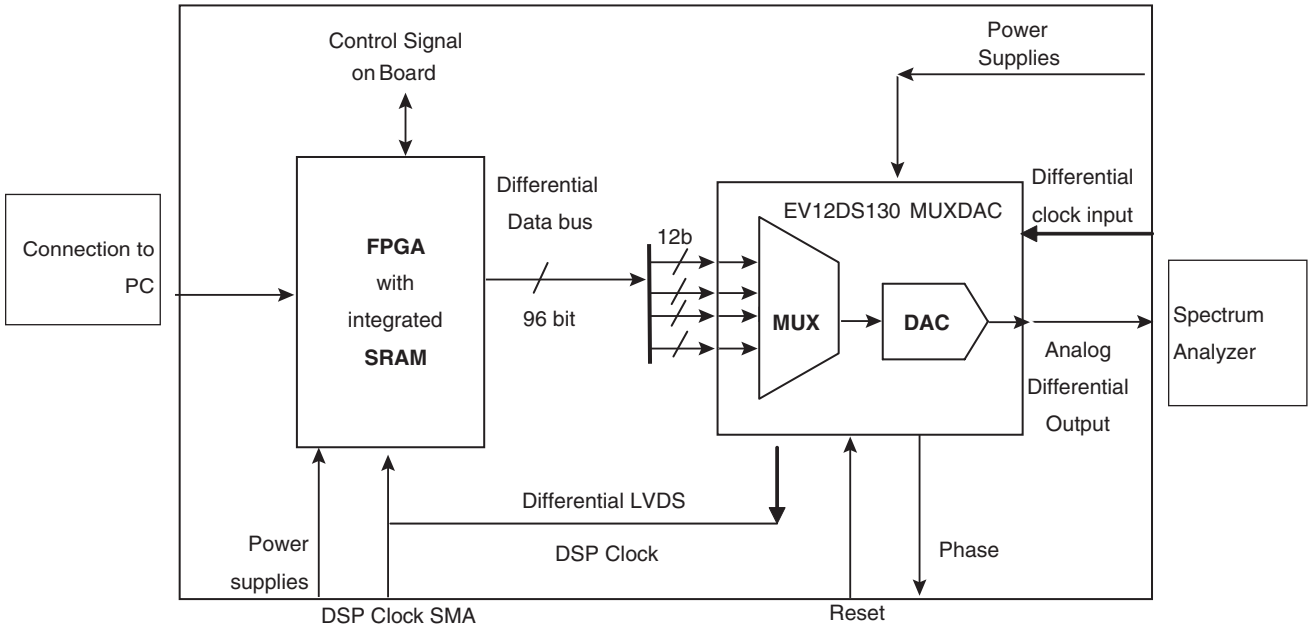
Thanks to its user-friendly interface, the EV12DS130ZPY-EB Kit enables to test all the functions of the EV12DS130 12-bit MUXDAC.

To achieve optimal performance, the EV12DS130ZPY-EB is designed in a 6-metal-layer board using RO4003 epoxy dielectric material. The board implements the following devices:

- The EV12DS130 12-bit MUXDAC evaluation board with the EV12DS130 12-bit MUXDAC soldered
- SMA connectors for CLK, CLKN, OUT, OUTN, RESET, RESETN, PHASE, PHASEN, DSP, DSPN
- ALTERA FPGA soldered to generate the logical pattern
- Banana jacks for the power supply accesses, the die junction temperature monitoring functions, reference resistor
- An RS-232 connector for PC interface

The board dimensions are 180 mm x 210 mm. The board comes fully assembled and tested with the EV12DS130 installed.

Figure 1-1. EV12DS130-EB Evaluation Board Simplified Schematic



As shown in Figure 1-1, different power supplies are required:

- V_{CCA5} = 5V analog positive power supply
- V_{CCD} = 3.3V digital positive power supply
- V_{CCA3} = 3.3V analog output power supply
- 5V FPGA
- 1.2V FPGA

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Section 2

Hardware Description

2.1 Board Structure

In order to achieve optimum full-speed operation of the EV12DS130ZPY-EB 12-bit MUXDAC, a multi-layer board structure was retained for the evaluation board. Six copper layers are used, dedicated to the signal traces, ground planes and power supply planes.

The board is made in RO4003 dielectric material. Table 2-1 gives a detailed description of the board's structure.

Table 2-1. Board Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces
RO4003/dielectric layer	Layer thickness = 200 µm
Layer 2 Copper layer	Copper thickness = 18 µm Ground plane = AGND - DGND plane
RO4003/dielectric layer	Layer thickness = 350 µm
Layer 3 Copper layer	Copper thickness = 18 µm Power plane = FPGA supplies, VCCD, VCCA3, signals
RO4003/dielectric layer	Layer thickness = 350 µm
Layer 4 Copper layer	Copper thickness = 18 µm Reference plane = ground and power plane
RO4003/dielectric layer	Layer thickness = 350 µm
Layer 5 Copper layer	Copper thickness = 18 µm Power planes = DGND, V_{CCA5}, GA plane
RO4003/dielectric layer	Layer thickness = 200 µm
Layer 6 Copper layer	Copper thickness = 40 µm (with NiAu finish) AC signals traces = 50Ω microstrip lines DC signals traces

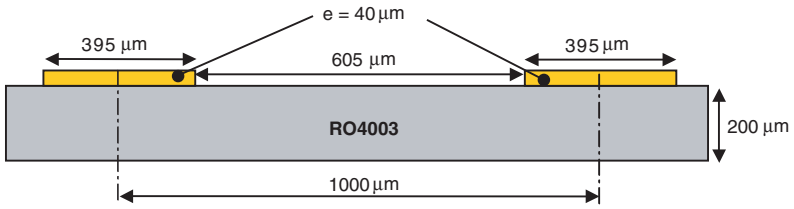
2.2 Analog Outputs

The differential analog output is provided by SMA connectors (reference: VITELEC 142-0701-8511). Both pairs are AC coupled using 100 nF capacitors. (Reference ATC545L Series UBC).

Special care was taken for the routing of the analog output signal for optimum performance in the high-frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between OUT and OUTN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the OUT and OUTN ball footprints

Figure 2-1. Board Layout for the Differential Analog and Clock Inputs



Note: The analog output is AC coupled with 100 nF very close to the SMA connectors.

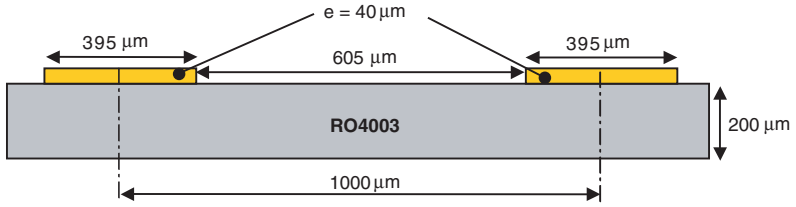
2.3 Clock Inputs

The differential clock inputs is provided by SMA connectors (reference: VITELEC 142-0701-8511). Both pairs are AC coupled using 100 pF capacitors.

Special care was taken for the routing of the clock input signal for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length) between CLK and CLKN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness
- 850 µm diameter hole in the ground layer below the CLK and CLKN ball footprints

Figure 2-2. Board Layout for the Differential Analog and Clock Inputs



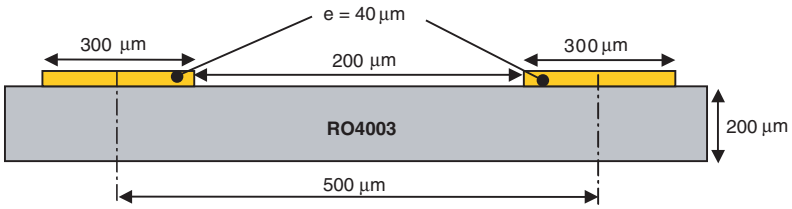
Note: The clock input is AC coupled with 100 nF very close to the SMA connectors.

2.4 Digital Inputs

The digital input lines were designed with the following recommendations:

- 50Ω lines matched to ±2.5 mm (in length) between signal of the same differential pair
- ±1 mm line length difference between signals of two differential pairs
- 500 µm pitch between the differential traces
- 650 µm between two differential pairs
- 300 µm line width
- 40 µm thickness

Figure 2-3. Board layout for the Differential Digital Inputs



The digital inputs are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

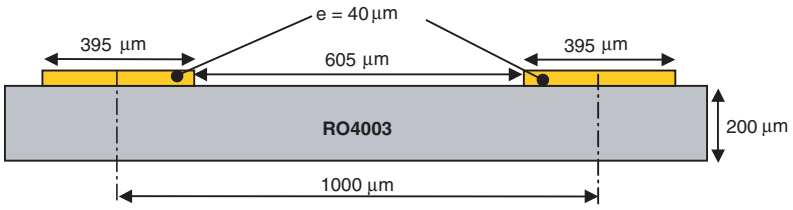
2.5 Reset Inputs

The hardware reset signals are provided; RESET, RESETN corresponds to the reset of the output of the DAC (analog reset).

The differential reset inputs are provided by SMA connectors (reference: VITELEC 142-0701-8511). The signals are AC coupled using 10 nF capacitors and pulled-up and pull-down resistors.

- 50Ω lines matched to ±0.1 mm (in length) between RESET and RESETN
- 605 µm pitch between the differential traces
- 1000 µm between two differential pairs
- 395 µm line width
- 40 µm thickness

Figure 2-4. Board Layout for the RESET Signal



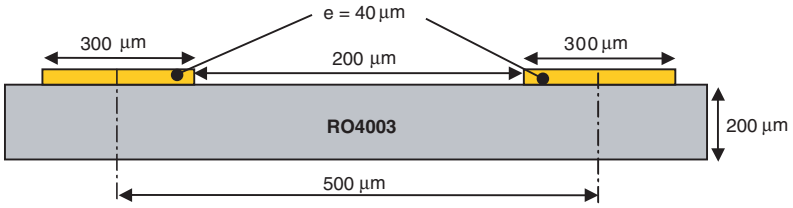
2.6 PHASE, PHASEN and DSP, DSPN Signals

The differential PHASE, PHASEN and DSP, DSPN signals are provided by the SMA connectors (reference: VITELEC 142-0701-8511).

Special care was taken for the routing of the PHASE, PHASEN and DSP, DSPN signals for optimum performance in the high frequency domain:

- 50Ω lines matched to ±0.1 mm (in length)
- 500 µm pitch between the differential traces
- 650 µm between two differential pairs
- 300 µm line width
- 40 µm thickness

Figure 2-5. Board layout for the PHASE, PHASEN and DSP, DSPN signals



This signals are compatible with LVDS standard. They are on-chip 100Ω differentially terminated.

DSP, DSPN and PHASE, PHASEN are not used for normal operation. They can be left open.

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2.7 Power Supplies

Layers 3, 4 and 5 are dedicated to power supply planes (V_{CCA3}, V_{CCD}, V_{CCA5}, 5V FPGA and 1.2V FPGA).

The supply traces are low impedance and are surrounded by two ground planes (layer 2 and 5).

Each incoming power supply is bypassed at the banana jack by a 1 µF Tantalum capacitor in parallel with a 100 nF chip capacitor. Each power supply is decoupled as close as possible to the EV12DS130 device by 10 nF in parallel with 100 pF surface mount chip capacitors.

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Section 3

Operating Characteristics

3.1 Introduction

This section describes a typical configuration for operating the evaluation board of the EV12DS130 12-bit MUXDAC.

The analog output signal and the sampling clock signal should be in a differential fashion.

Note: The analog outputs and clock inputs are AC coupled on the board.

3.2 Operating Procedure

1. Install the SPI software as described in section 4 “Software Tools”.
2. Connect the power supplies and ground accesses through the dedicated banana jacks.
   V_{CCA3} = 3.3V, V_{CCD} = 3.3V, V_{CCA5} = 5V and for the FPGA +5V and 1.2V
   Power supply +5V: 0.8A typical
   Power supply +1.2V: 1.2A typical
3. Connect the clock input signals. The clock input level is typically 3 dB to 10 dBm and should not exceed 12 dBm (into 50Ω).
4. Connect the analog output signals to a spectrum analyzer (the board has been designed to allow only AC coupled analog outputs). The analog output signals must be used in differential via differential-to-single transformer.
5. Connect the PC's RS-232 connector to the Evaluation Board's serial interface.
6. Switch on the DAC power supplies (recommended power-up sequence: simultaneous or in the following order: V_{CCA5} = 5V, V_{CCA3} = 3.3V, V_{CCD} = 3.3V then 5V FPGA and 1.2V FPGA).
7. Turn on the RF clock generator.
8. Perform an analog reset on the device (RESET/RESETN).
9. Launch the software, (the software must be launched with the evaluation board powered on).

The EV12DS130ZPY-EB evaluation board is now ready for operation.

3.3 Electrical Characteristics

For more information, please refer to the device datasheet.

Table 3-1. Recommended conditions of use

Parameter	Symbol	Comments	Recommended Value	Unit
Positive analog supply voltage	V_{CCA5}		5	V
Positive analog supply voltage	V_{CCA3}		3.3	V
Positive digital supply voltage	V_{CCD}		3.3	V
Digital inputs (on each single-ended input) V_{IL} V_{IH} Swing	A0..A11, A0N..A11N B0..B11, B0N..B11N C0..C11, C0N..C11N D0..D11, D0N..D11N		 1.075 1.425 350	
Master clock input	CLK, CLKN		1.2	Vpp
Master clock input power level (single-ended mode)	P_{CLK}		6	dBm
Control functions inputs	MUX, CS, RTZ, JIT	V_{IL} V_{IH}	0 V_{CCD}	V
Gain adjustment function	GA		V_{CCA3} /2 ± 0.5	V
Reset function	RESET, RESETN		1.075 1.425 350	
Operating temperature range	T_{amb}	Commercial *C* grade Industrial *V* grade Military *M* grade	0°C < T_{amb} < 70°C –40°C < T_{amb} < 85°C –55°C < T_{amb} <125°C	°C
Storage temperature	Tstg		–55 to 150	°C

Table 3-2. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Resolution		12			bit
ESD classification		TBD			
Power requirements					
Power supply voltage Analog Analog Digital	 V_{CCA5} V_{CCA3} V_{CCD}	 4.75 3.15 3.15	 5 3.3 3.3	 5.25 3.45 3.45	 V V
Power supply current Analog Analog Digital	 I_{CCA5} I_{CCA3} I_{CCD}		 59 153 136		 mA mA mA
Power dissipation (4:1 MUX)	P_D		1.25		W
Power dissipation (2:1 DMUX)	P_D		1.18		W

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Section 4

Software Tools

4.1 Overview

The MUXDAC 12-bit evaluation user interface software is a Visual C++ compiled graphical interface that does not require a licence to run on a Windows NT and Windows 2000/98/XP PC.

The software uses intuitive push-buttons and pop-up menus to write data from the hardware.

4.2 Configuration

The advised configuration for Windows 98 is:

- PC with Intel Pentium Microprocessor of over 100 MHz
- Memory of at least 24 Mo.

For other versions of Windows OS, use the recommended configuration from Microsoft.

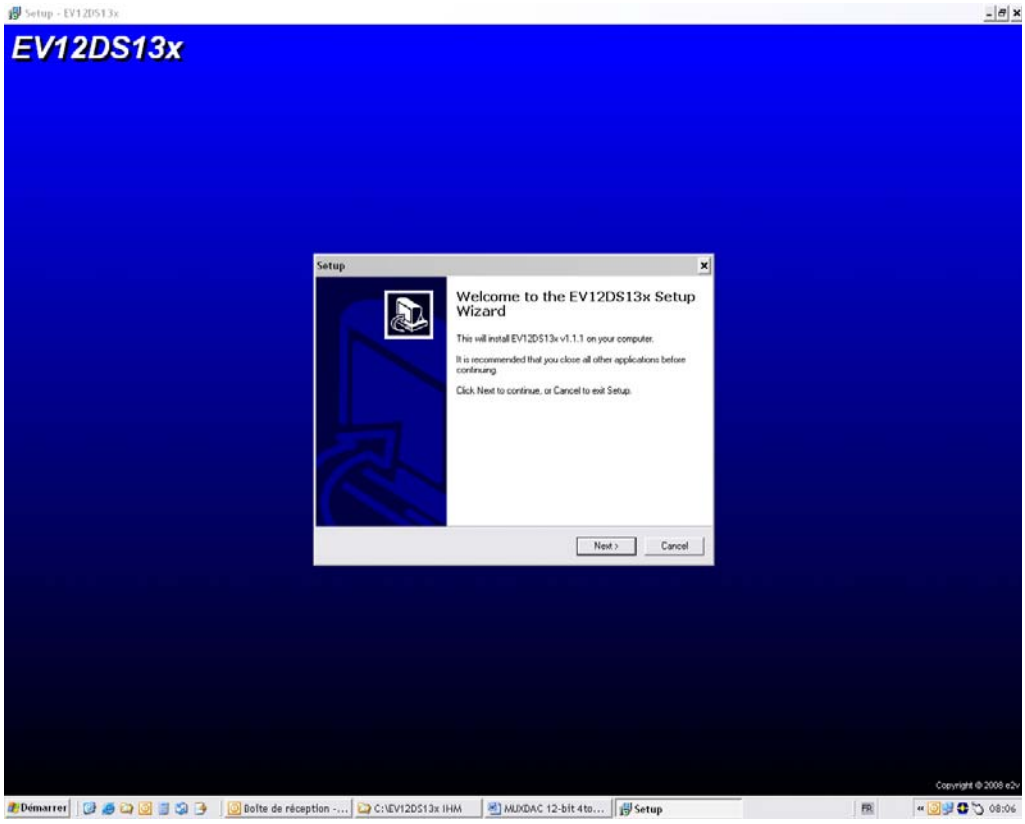
Note: Two COM ports are necessary to use two boards simultaneously.

4.3 Getting Started

1. Install the 12-bit MUXDAC application on your computer by launching the Setup_EV12DS13x_1.exe installer (please refer to the latest version available).

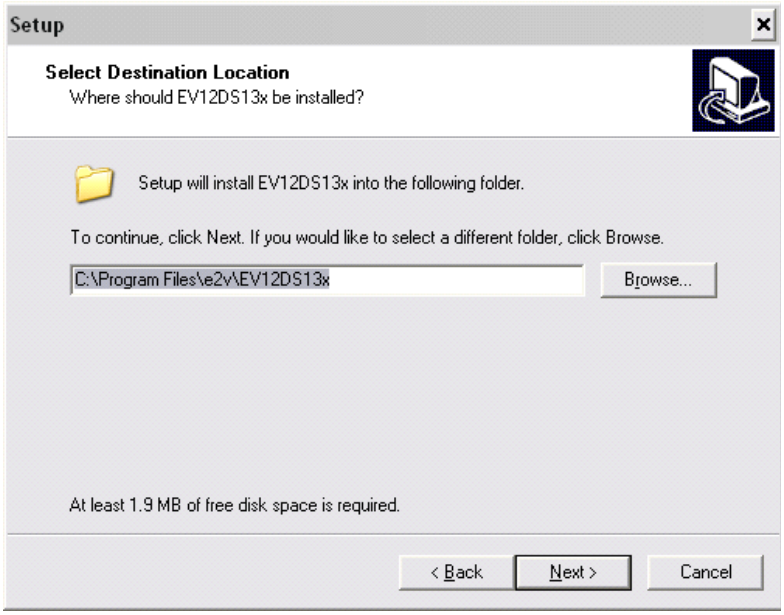
The screen shown in Figure 4-1 is displayed:

Figure 4-1. Application *Setup Wizard* Window



2. Select Destination Directory

Figure 4-2. *Select Destination Directory* Window

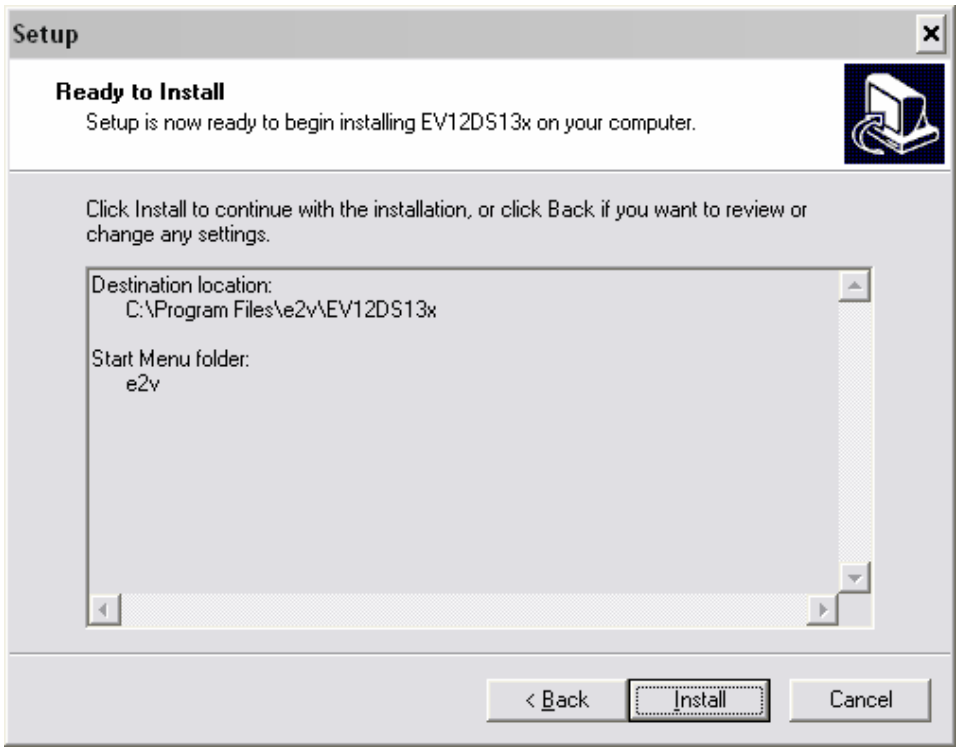


3. Select Start Menu Folder

Figure 4-3. Select *Start Menu* Window

1. Ready to install

Figure 4-4. *Ready to Install* Window

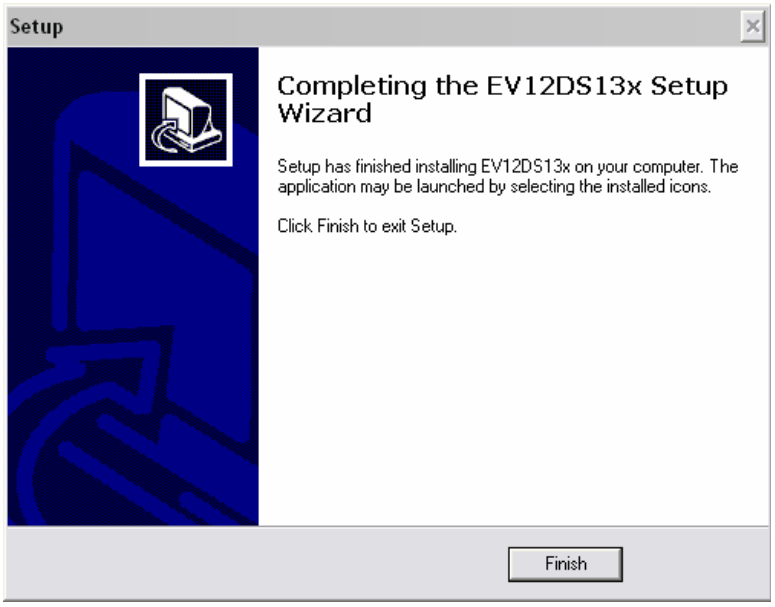


If you agree with the install configuration, press **Install**.

Figure 4-5. Install Button

The installation of the software is now completed.

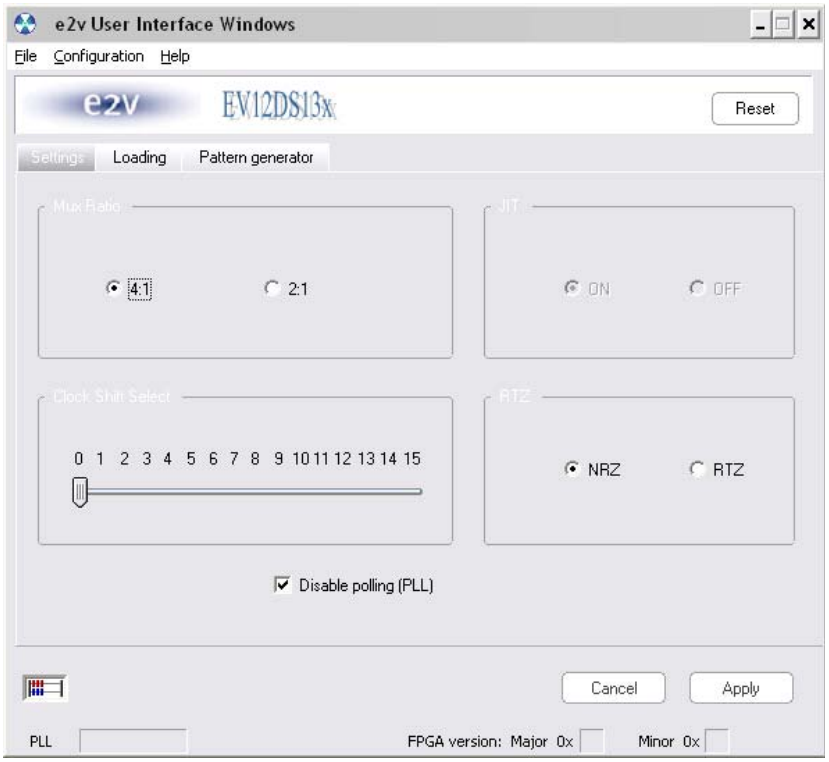
Figure 4-6. Completing *Setup Wizard* Window



After the installation, you can launch the interface with the following file: C:\Program Files\e2v\...

The window shown in Figure 4-7 will be displayed.

Figure 4-7. User Interface Window



Notes:
1. If the MUXDAC application board is not connected or not powered, an error message is displayed.
2. Check your connection and restart the application (refer to section 3).

4.4 Troubleshooting

1. Check that you own rights to write in the directory.
2. Check for the available disk space.
3. Check that at least one RS-232 serial port is free and properly configured.
4. Check that the serial port and DB9 connector are properly connected.
5. Check that all supplies are properly powered on.

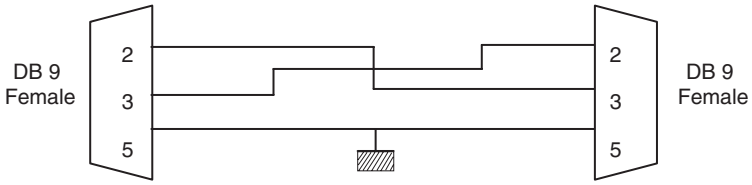
The serial port configuration should be as follows:

- Bit rate: 19200
- Data coding: 8 bits
- 1 start bit, 1 stop bit
- No parity check

Figure 4-8. User Interface Hardware Implementation

1. Use an RS-232 port to send data to the DAC.
2. Connect the crossed DB9 (F/F) cable between your PC and your evaluation board as illustrated in Figure 4.9.

Figure 4-9. Crossed Cable



4.5 Operating Modes

The MUXDAC software included with the evaluation board provides a graphical user interface to configure the DAC.

Push buttons, popup menus and capture windows allow easy:

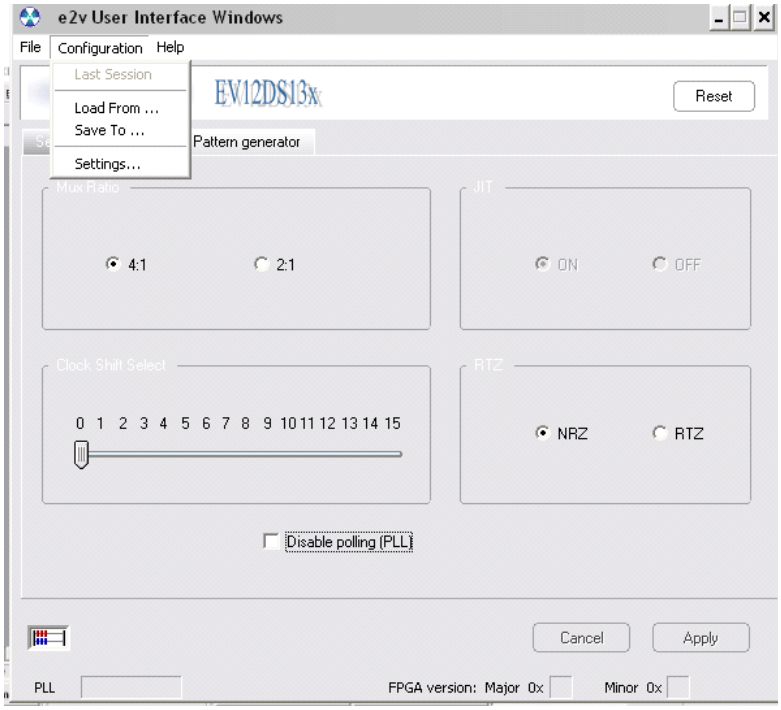
With Setting and Test mode windows always click on *Apply* button to validate any command.

Figure 4-10. Cancel/Apply Buttons

Clicking on the *Cancel* button will restore last settings sent with *Apply* button.

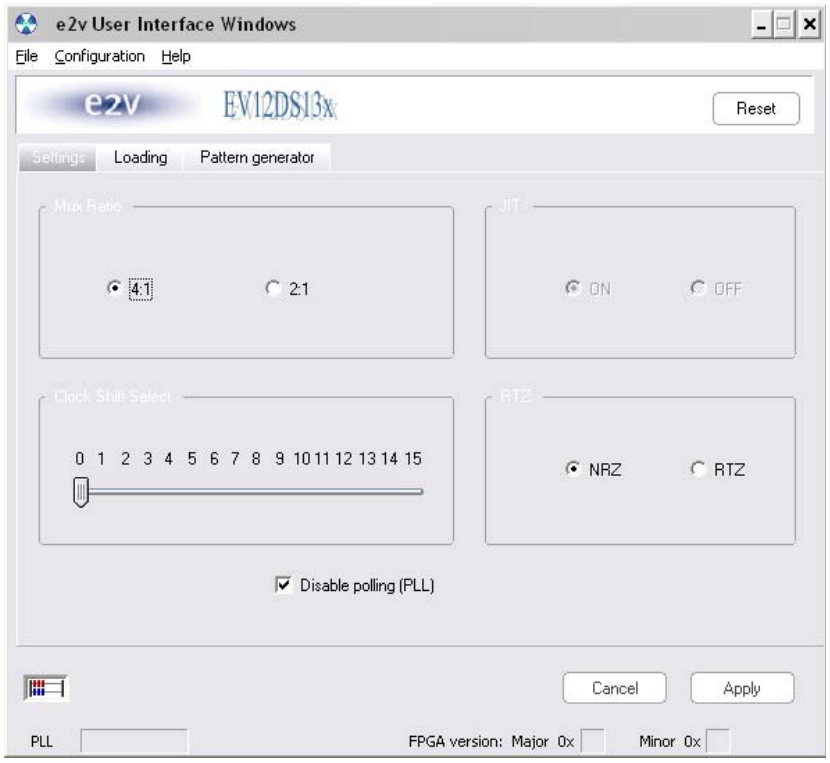
The user might *Save* or *Load* the register configuration via the configuration function.

Figure 4-11. Save/Load Register Configuration Window



4.5.1 Settings

Figure 4-12. Settings Window



The software allows choosing between the MUX ratio 2 to 1 or 4 to 1.

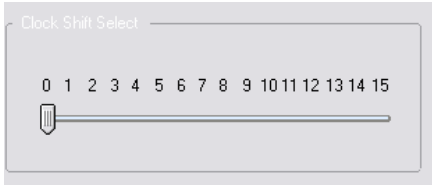
Figure 4-13. MUX Ratio

DAC MUX ratio could be set to 4:1 or 2:1:

- In 2:1 configuration of the clock speed is limited up to 1.5 GHz
- In 4:1 configuration of the clock speed is limited up to 3.0 GHz

The software allows adjusting the *Clock shift Select* delay to avoid a forbidden area between the data input and the clock input.

Figure 4-14. Clock Shift Select



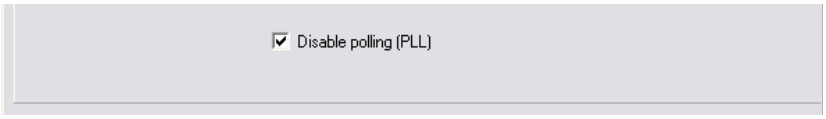
The function allows to shift the DSP clock. In normal use it is not necessary to change the *Clock Shift Select* setting. In case of acquisition time issue between the FPGA and

the DAC (vs. clock frequency), this *Clock Shift Select* function should allow to align the DAC to the FPGA; adjust the *Clock Shift Select* until the acquisition is correct.

Figure 4-15. Non-return-to-zero Mode Window

– NRZ allows to work in first Nyquist zone only
– RTZ allow to work at first and second Nyquist zone

Figure 4-16. PLL Disable



The polling function allows to scan the FPGA to know the FGPA version and the PLL state.

Figure 4-17. PLL Locked

4.5.2 Loading

This module allows to send the pattern to the MUXDAC.

You can choose to send a ramp pattern or to send a dedicated pattern.

For ramp pattern:

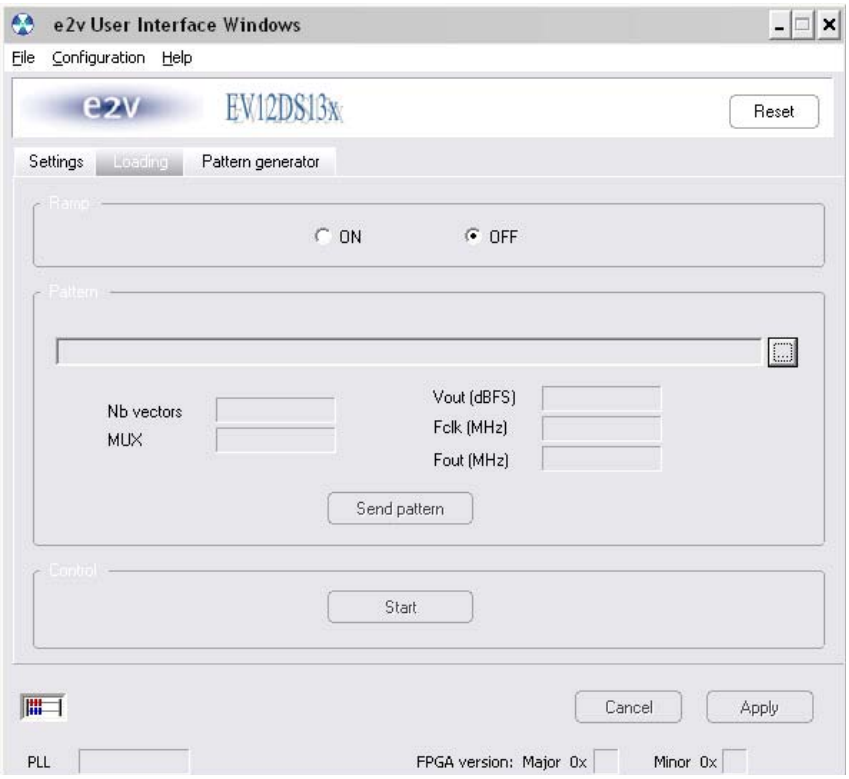
- Active *Ramp* ON
- Press **Start** (for stop press **Stop**)

For dedicated pattern:

- Find the pattern file in the folders' architecture
- Check the information (nb vectors, MUX etc.)
- Press **Send** pattern
- Press **Start**
- For stop pattern press **Stop**

Note: Before loading new pattern press *Stop*

Figure 4-18. Loading Process Window



4.5.3 Pattern Generator

This module allows creating sinewave pattern file only in order to send the data to the MUXDAC.

Pattern generator procedure:

- Enter information for each field
  - Vout: level of output signal in dBFS
  - Fclk: frequency of clock input signal
  - Fout: frequency of output signal
  - Number of vectors = number of data sent to DA

    Vector minimum = 8

    Vector maximum = 32767
  - The number of vectors should be a multiple of 8
  - MUX: Selectable MUX ratio

    1 for DMUX 2:1

    2 for DMUX 4:1
- Give the path of the target folder to save the pattern
- Click on *create pattern*

Figure 4-19. Pattern Generator Window

If you wish to create your own pattern file, please make sure to follow the below example.

Example of Pattern file

```
# Vout (dBFS)     -6
# Fclk (MHz)      2000
# Fout (MHz)      2430.05
# MUX             2    DMUX4:1
# Nb vectors      4096
#
Vector 0:    100000000000  101111101001  100110110100  010011010100
Vector 1:    010011101001  100111010010  101111100001  011111011110
Vector 2:    010000001111  011001101001  101100111111  101100000000
Vector 3:    011000001111  010000100110  100001000010  101111110110
Vector 4:    100101110111  010010101101  010100010101  101000001101
Vector 5:    101111001111  011110011011  010000000101  011010101000
Vector 6:    101101100100  101011010010  010111010110  010000111011
.............................................................
.....................................................................
..................................................................... etc
Vector 4089:    011110000001  101111000101  101000101011  010100110001
Vector 4090:    010010011101  100101011000  101111111011  100001011101
Vector 4091:    010000110000  010111110001  101011100101  101101010000
Vector 4092:    011010001000  010000001001  011111000011  101111011001
Vector 4093:    100111110010  010100000011  010011000011  100110010110
Vector 4094:    101111110001  100000011011  010000011101  011000101011
Vector 4095:    101100010010  101100101000  011001001011  010000010101
```

4.6 Configuration and Software of the FPGA Memory

4.6.1 PROG FPGA

The configuration of the FPGA memory is done via the connector *PROG FPGA* already soldered on the evaluation board.

The schematic is shown in figure 4-20.

Figure 4-20. FPGA Configuration in AS Mode (Serial Configuration Device Programmed Using Download Cable)

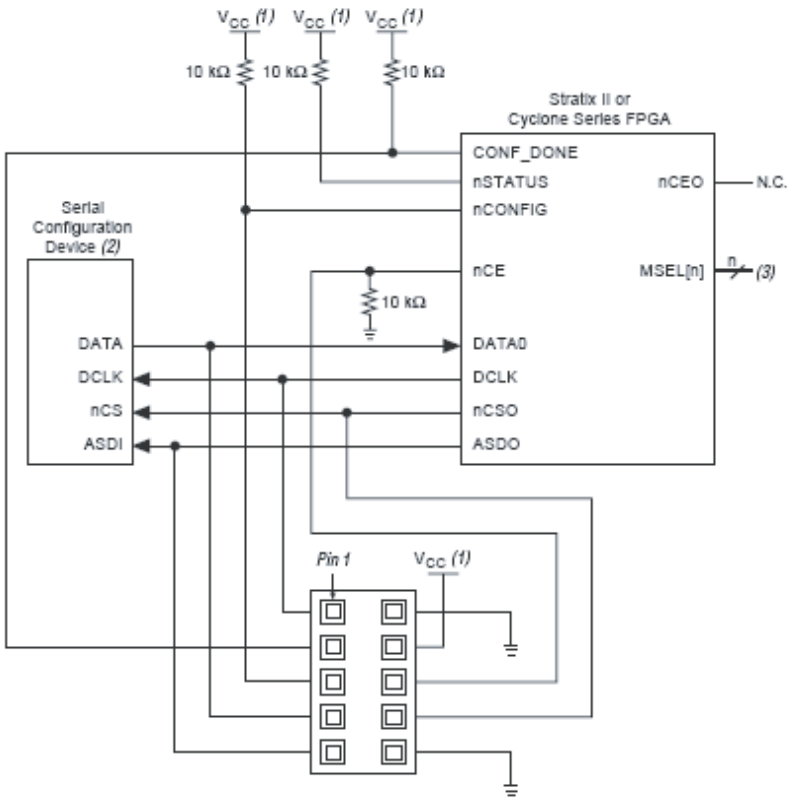


Table 4-1. Connector Type HE10 Male 2x5 points

Pin	Name	Pin	Name
1	DCLK (Serial clock)	2	GND (ground)
3	CONF-DONE (pull-up VCC)	4	VCC = 3.3V
5	nCONFIG (pull-up VCC)	6	nCE (pull-down)
7	DATA0 (data prog FPGA)	8	nCSO (Chip select)
9	ASDO	10	GND (ground)

For the configuration of the serial memory, there is a 4-bit configuration (MSL0-3).

In this application note that we use the FAST AS (40 MHz) mode:

- MSEL3: jumper out
- MSEL2: jumper in
- MSEL1: jumper in
- MSEL: jumper in

Table 4-2 shows the MSEL pin settings when using the AS configuration scheme.

Table 4-2. STRATIX II and STRATIX II gx MSEL Pin Settings for AS Configuration

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSLE0
Fast AS (40 MHz)(1)	1	0	0	0
Remote system upgrade fast AS (40 MHz)	1	0	0	1
AS (20 MHz)(1)	1	1	0	1
Remote system upgrade AS (20 MHz)(1)	1	1	1	0

Note: 1. Only the EPCS16 and EPCS64 devices support a DCLK up to 40 MHz clock; other EPCS devices support a DCLK up to 20 MHz.

4.6.2 FPGA Configuration with JTAG

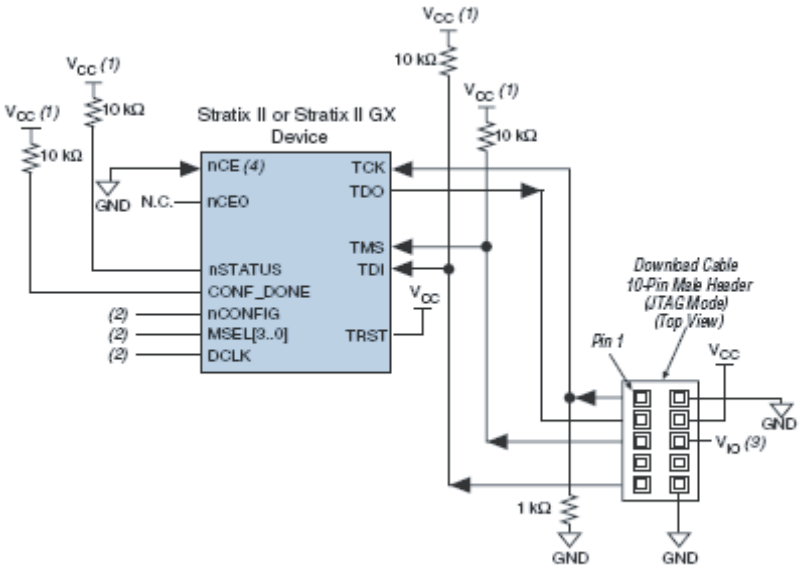
FPGA configuration with JTAG is used on debug mode.

Note: If the evaluation is powered off, the FPGA loses its configuration

The programming is implemented via JTAG connector. This connector is not on the evaluation board.

The schematic is shown in figure 4-21.

Figure 4-21. Configuration of a Single Device Using a Download Cable



Notes:
1. The pull-up resistor should be connected to the same supply voltage as the USB Blaster, MasterBlaster V_{10} pin byteBlasterII or ByteBlasterMV cable.
2. The jumper configuration (MSEL) has no effect in this mode.

4.6.3 Configuration of the FPGA on EV12DS130ZPY Evaluation Board

This sequence is correct for the serial memory configuration and JTAG configuration.

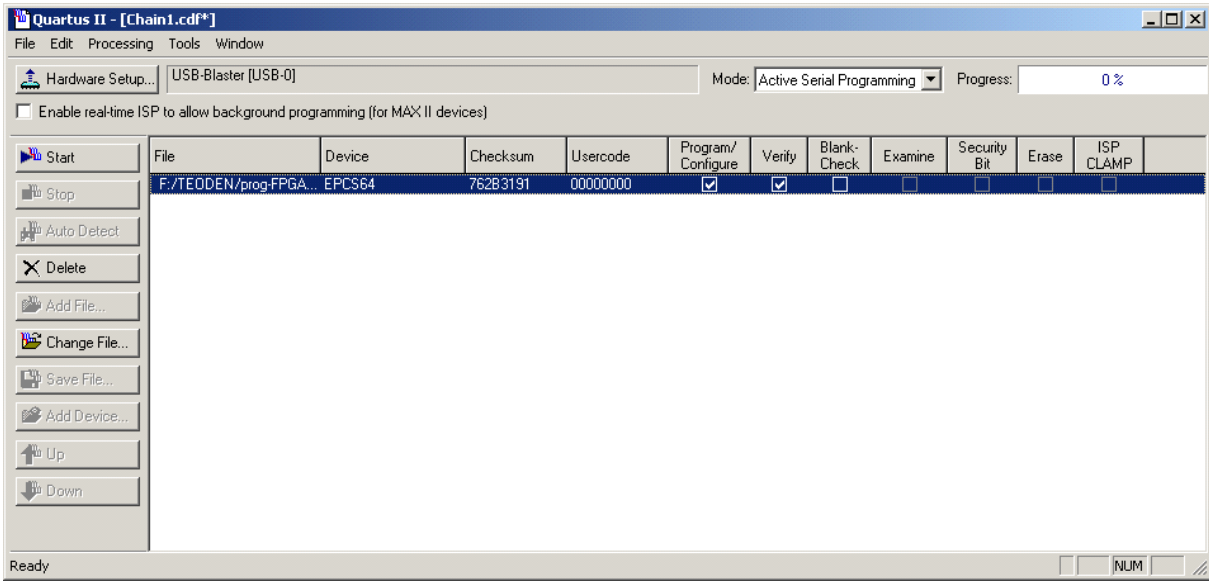
Sequence:

1. Setup the power supplies +5V and +1.2V
2. Connect the jumper MSEL (only for the serial memory)
   - MSEL3: Jumper off (signal to 3.3V)
   - MSEL2, MSEL1, MSEL0: jumper on (signal to GND)
   - RAMP _PATTERN: no jumper
3. Connect the USB BLASTER ALTERA cable on the evaluation board
   - PROG FPGA: for serial memory configuration
   - JTAG: For the JTAG configuration
4. Switch ON the supplies
   - First 1V2, then 5V
5. Launch ALTERA QUARTUS II 8.0 software
6. Click on **Program**.

The window shown in figure 4-22 is displayed:

7. Check that the *USB blaster [USB-0]* is selected, or click on *Hardware Setup* to perform this.
8. Select the mode *Active Serial Programming* for the serial memory programming.
9. Select the mode JTAG for programming via JTAG
10. Choose the program file (teoden_top.pof design 3 GHz) via *Add file*. The information must be indicated.
11. Click on **Start** to launch the program.

Figure 4-22. Sequence Serial Memory Configuration and JTAG Configuration



The FPGA configuration is complete when the *Progress* status shows 100%. For the serial memory mode, switch off the 5V supply first, then the 1V2.

12. Disconnect the USB BLASTER ALTERA cable, then power up the evaluation board to load the software via the external serial memory.

Section 5

Application Information

5.1 Analog Outputs

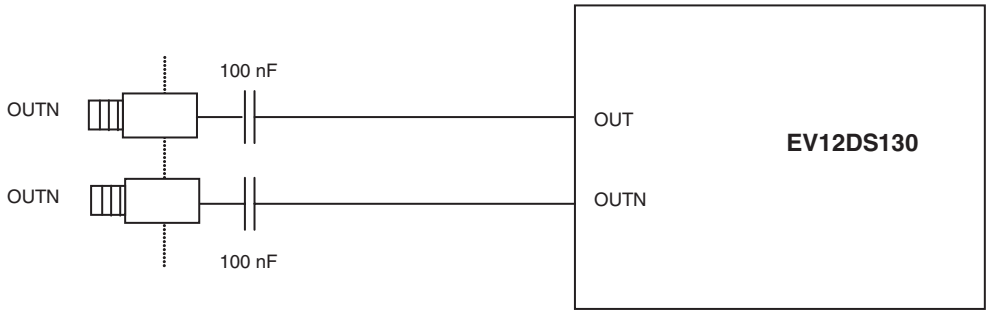
The analog output is in differential AC coupled mode as described in Figure 5-1.

The single-ended operation for the analog output is allowed but it may degrade the DAC performance significantly. It is therefore recommended to use a differential via an external balun or differential amplifier.

Note: References of differential amplifiers and external baluns:

- M/A-COM H9 balun
- M/A-COM TP101 1:1 transformer
- ANAREN 3A0056 3 dB coupler 2G-4G
- KRYTAR double arrow 180° hybrid 2G-8G

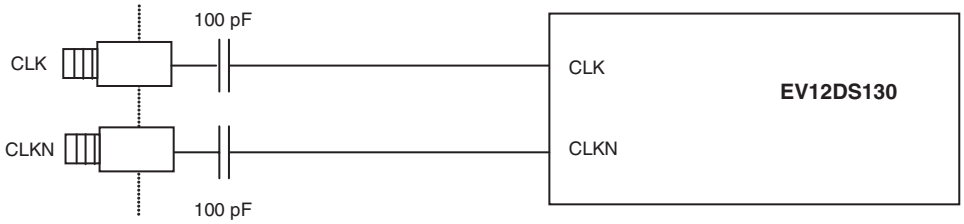
Figure 5-1. Differential Analog Output Implementation



5.2 Clock Inputs

The clock input can be entered indifferently in single-ended or differential mode with no performance degradation. The clock is AC coupled via 100 pF capacitors as described in Figure 5-2.

Figure 5-2. Clock Input Implementation



5.3 RESET Inputs

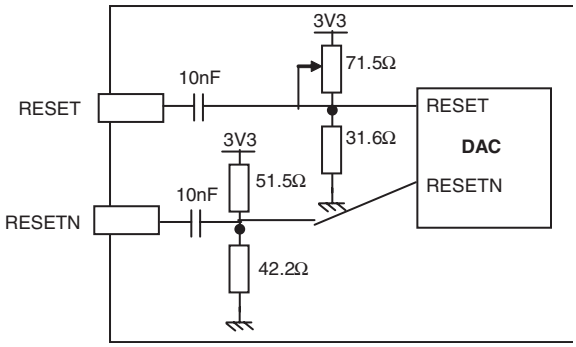
The RESET, RESETN is necessary to start the DAC after power up.

The reset signal is implemented as illustrated in Figure 5-3. There are two methods of applying a RESET:

– Either use the potentiometer

– Or apply a square LVDS signal on RESET, RESETN

Figure 5-3. RESET RESETN Inputs Implementation

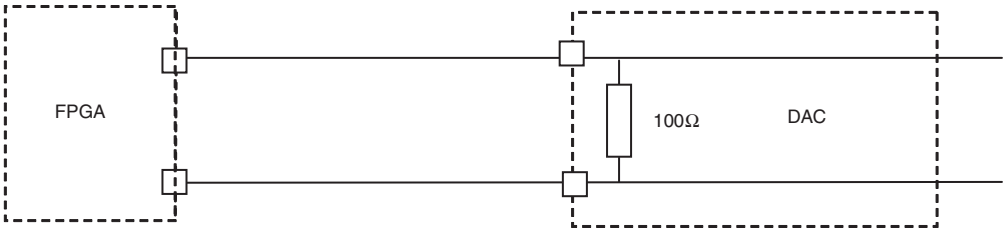


5.4 Input Data

The input data are LVDS differential and are 100Ω on chip terminated to ground as shown in Figure 5-4.

The input data of DAC is generated by the FPGA.

Figure 5-4. Input Data on-board Implementation

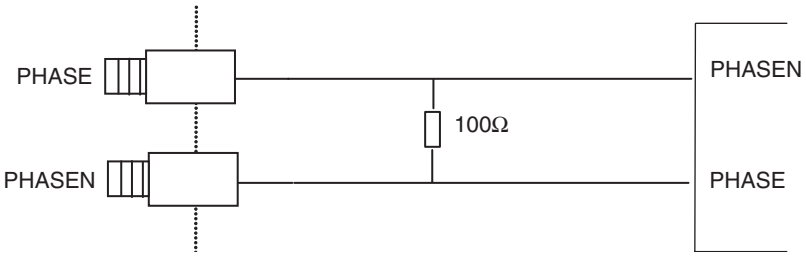


0989B–BDC–12/09

5.5 PHASE, PHASEN

The PHASE, PHASEN output is accessed via SMA connector and is 100Ω differentially terminated.

Figure 5-5. PHASE, PHASEN Implementation

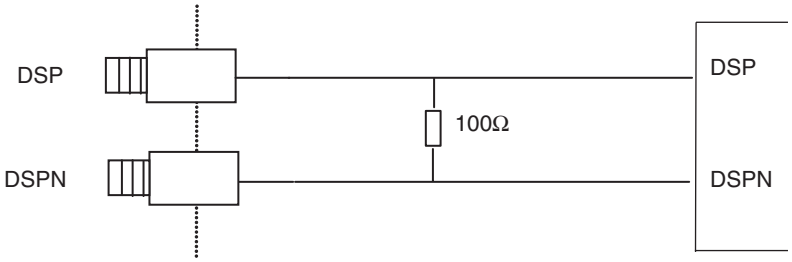


This signal can be used to determine if the digital input data and the sampling clock are internally in phase in the DAC. Please refer to the device datasheet for more explanations (reference 0954).

5.6 DSP, DSPN Signal

The DSP, DSPN output signal is accessed via SMA connector and is 100Ω differentially terminated.

Figure 5-6. DSP, DSPN Implementation



The DSP output clock is used to synchronize the FPGA generating the digital patterns with the DAC sampling clock. Please refer to the device datasheet for more information (reference 0954).

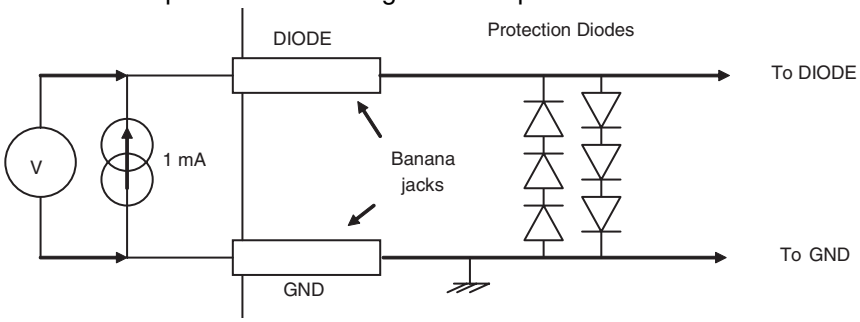
5.7 Diode for Junction Temperature Monitoring

Two banana jacks of 2 mm are provided for the die junction temperature monitoring of the DAC.

One banana jack is labeled DIODE and should be applied with a current of up to 1 mA (via a multimeter used in current source mode) and the second one is connected to GND. The DAC diode is protected via 2 x 3 head-to-tail diodes.

Figure 5-7 describes the setup for the die junction temperature monitoring using a multimeter.

Figure 5-7. Die Temperature Monitoring Test Setup



Section 6

Ordering Information

Table 6-1. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
EVX12DS130ZPY	fpBGA916 RoHS	Ambient	Prototype	
EV12DS130ZPY-EB	fpBGA916 RoHS	Ambient	Prototype	Evaluation board

Section 7

Appendices

7.1 EV12DS130ZPY-EB Electrical Schematics

Figure 7-1. Power Supplies Bypassing

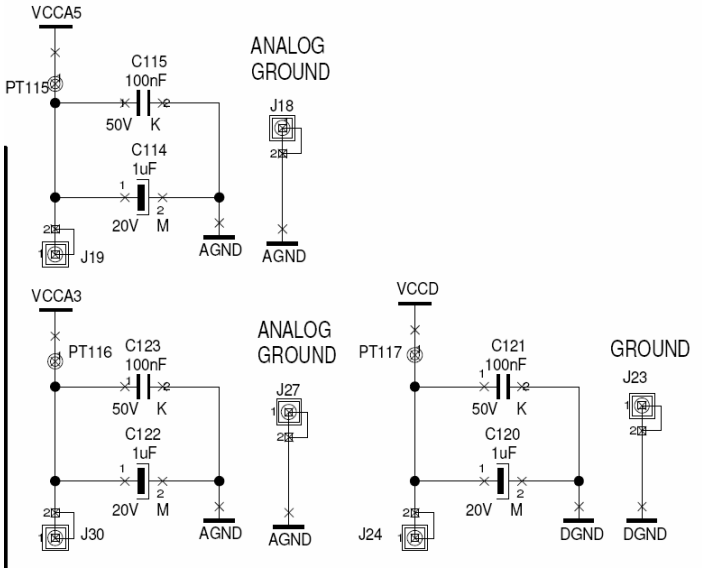


Figure 7-2. Power Supplies Decoupling (J = ±5% tolerance)

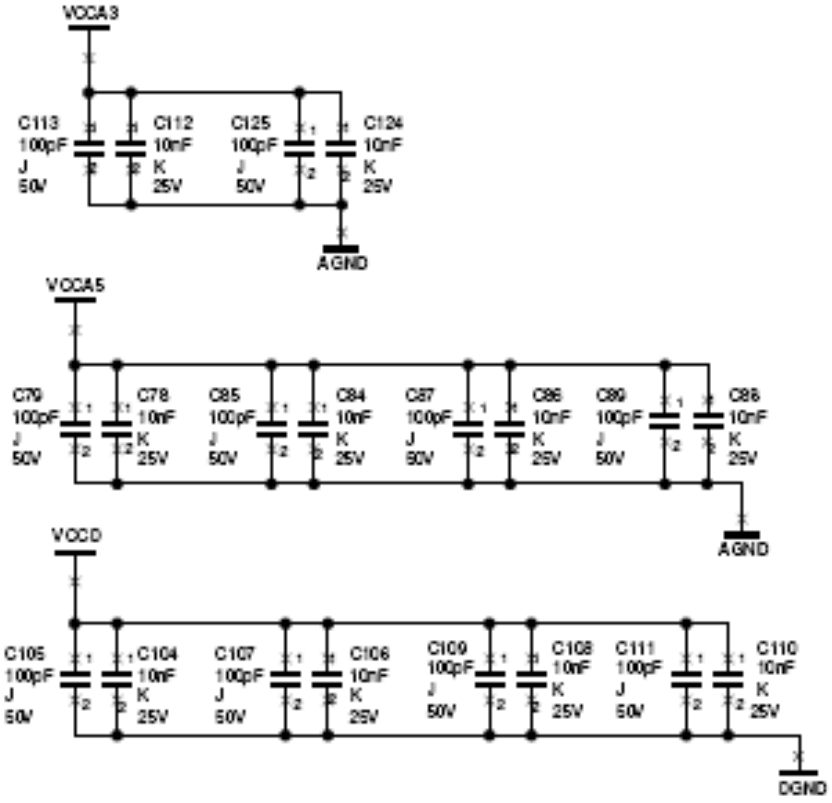


Figure 7-3. Electrical Schematics (DAC)

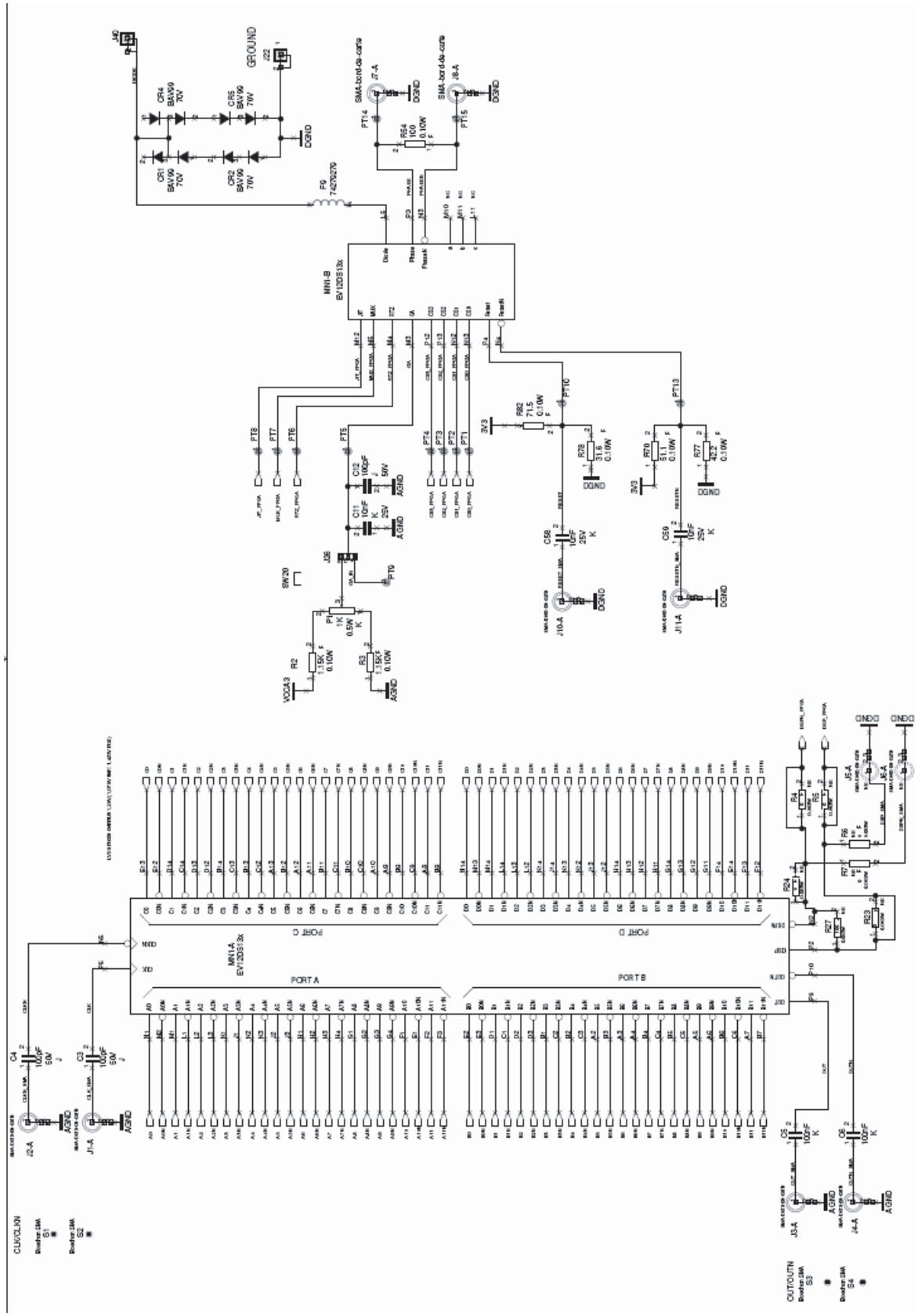


Figure 7-4. EV12DS130ZPY-EB Board Layers

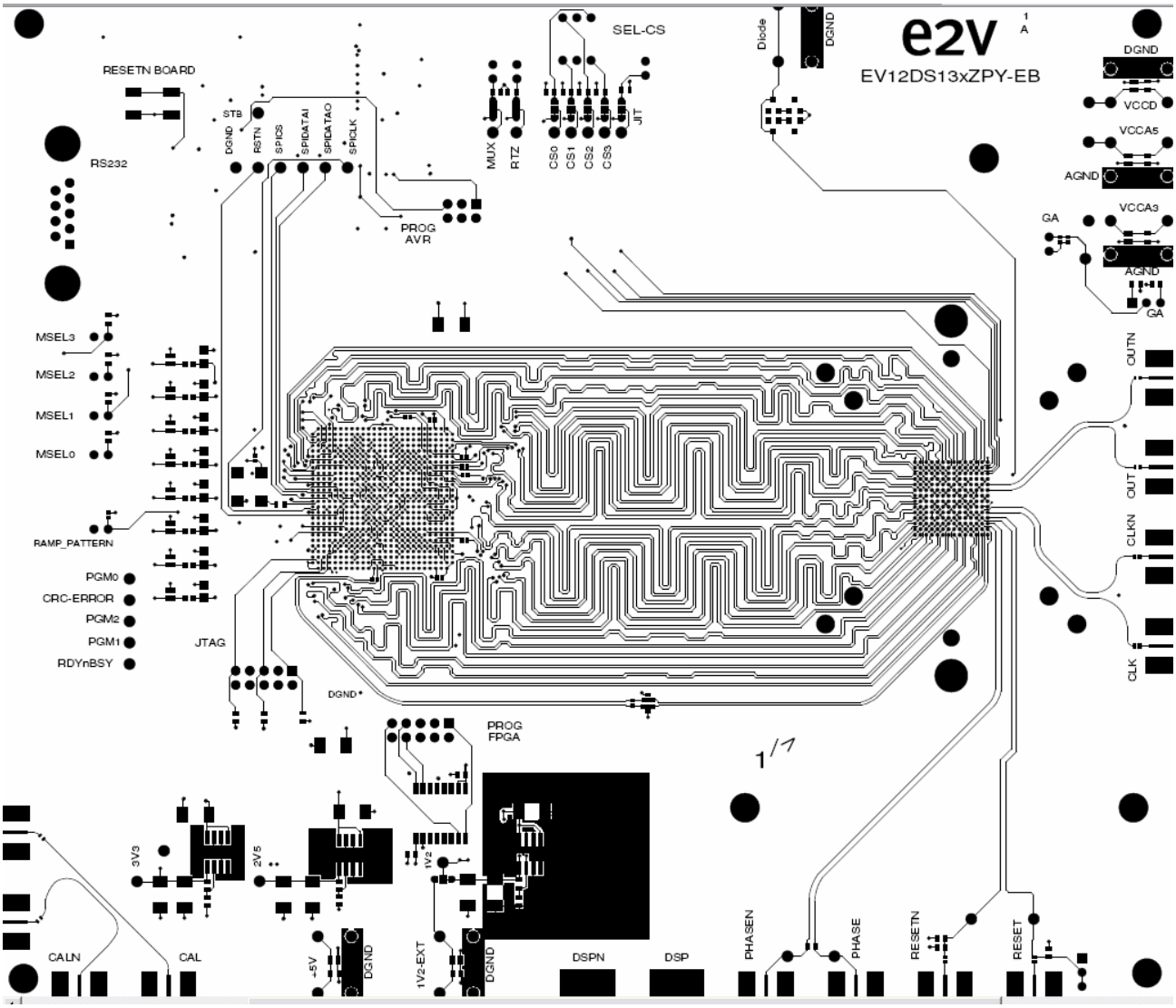


Figure 7-5. Bottom Layer

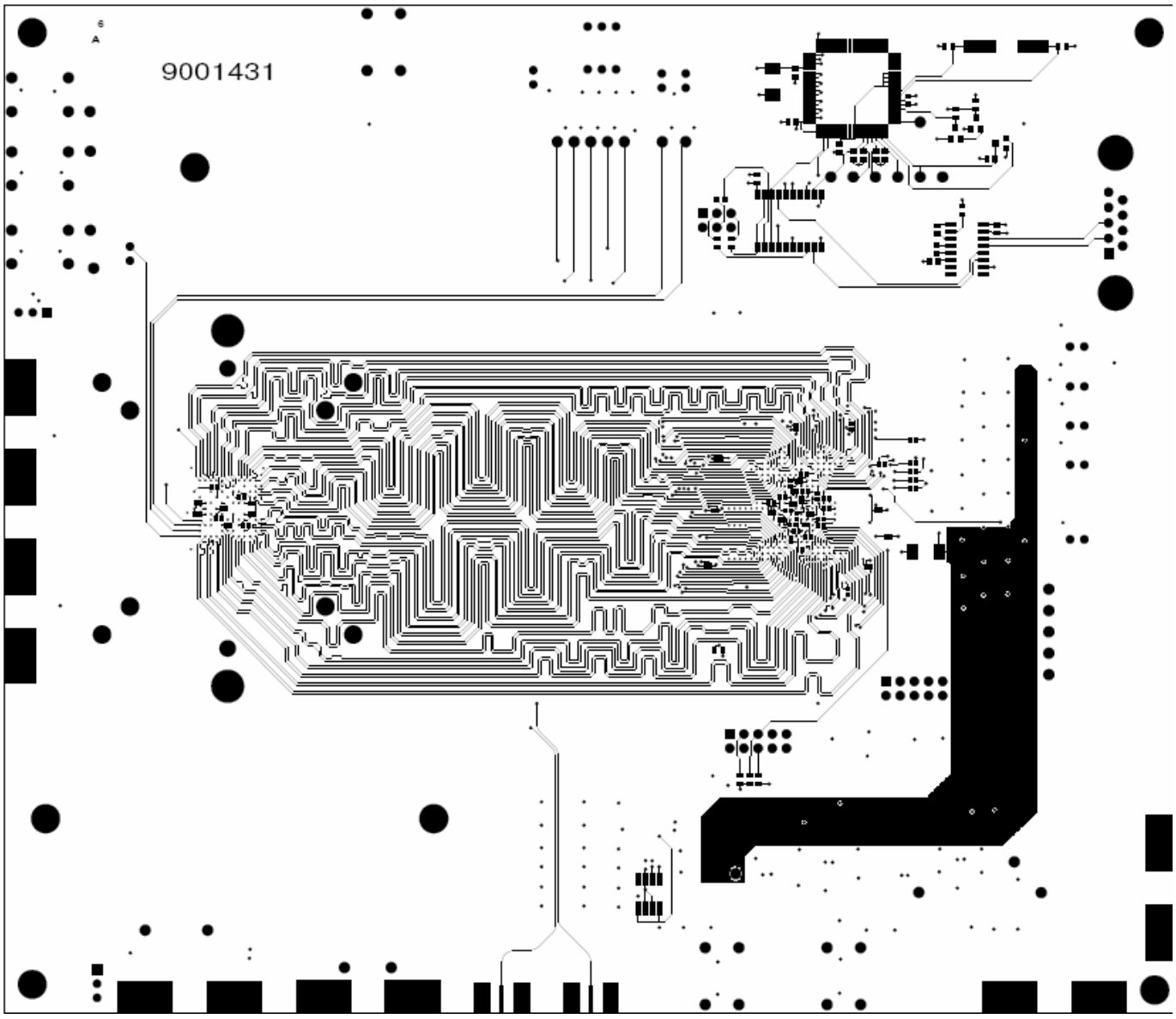
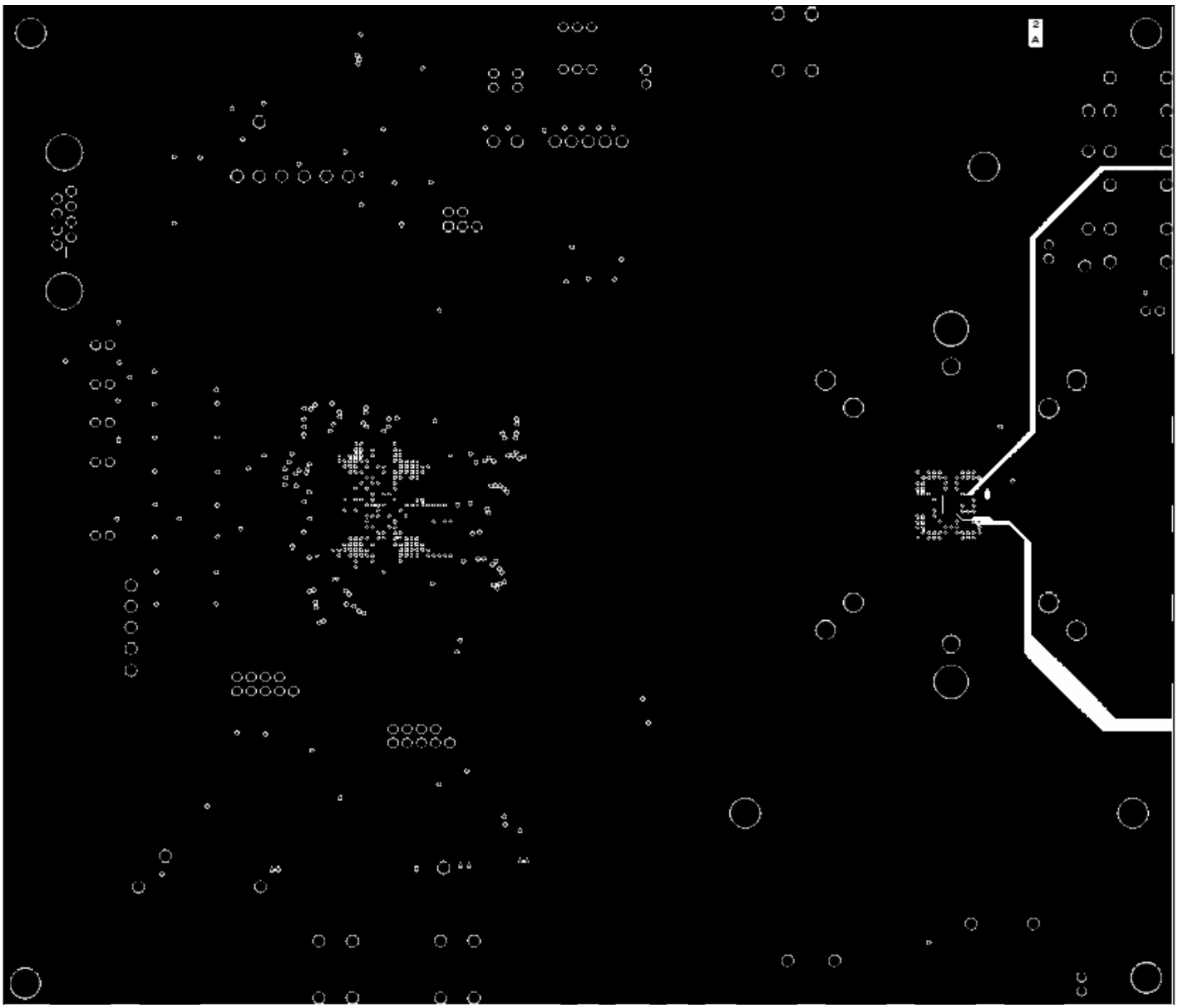
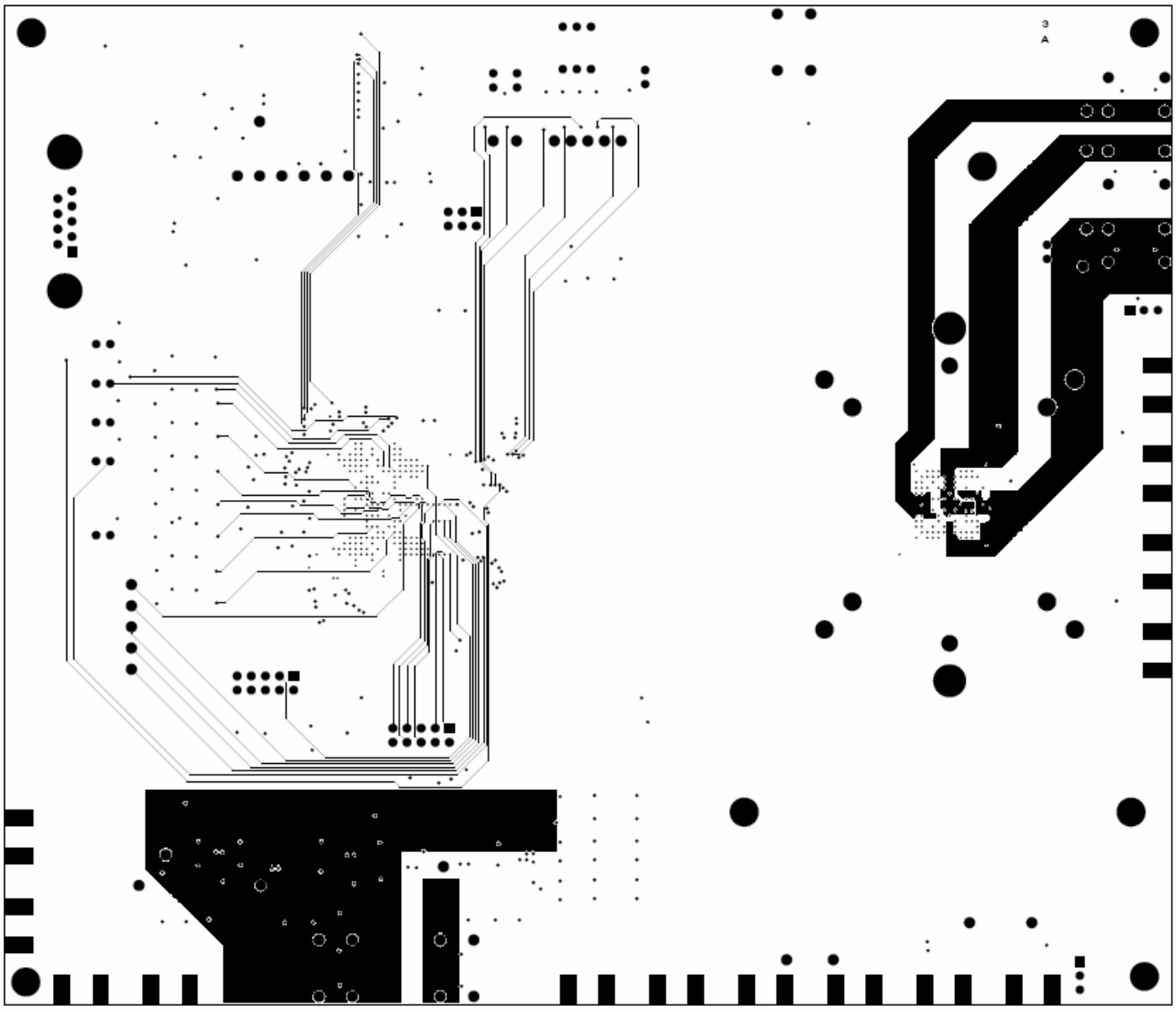


Figure 7-6. Layer 2 GND Plane



0989B–BDC–12/09

Figure 7-7. Layer 3 Power Supplies



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