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10-bit 2.2 Gsps ADC Evaluation Board - AT84AS008-EB

User Guide

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Section 1
Overview

1.1 Description

The AT84AS008-EB Evaluation Board is a prototype board which has been designed to facilitate the evaluation and characterization of the AT84AS008 device (in CBGA152) up to its 3.3 GHz full power bandwidth at up to 2.2 Gsps in the extended temperature range.

The high speed of the AT84AS008 requires that careful attention be paid to the circuit design and layout so as to achieve the optimal performance. This six metal layer board with an internal ground plane offers functions that enable a quick and simple evaluation of the AT84AS008 ADC's performances over the temperature range.

The AT84AS008 Evaluation Board (EB) is very straightforward as it only implements the AT84AS008 ADC device, SMA connectors for input/output accesses and a 2.54 mm pitch connector compatible with high-speed acquisition system high-frequency probes.

The board has been designed for full compatibility with e2v's DMUX evaluation boards (AT84CS001-EB). Please refer to user guide reference 0904 and datasheet reference 0809 for more information.

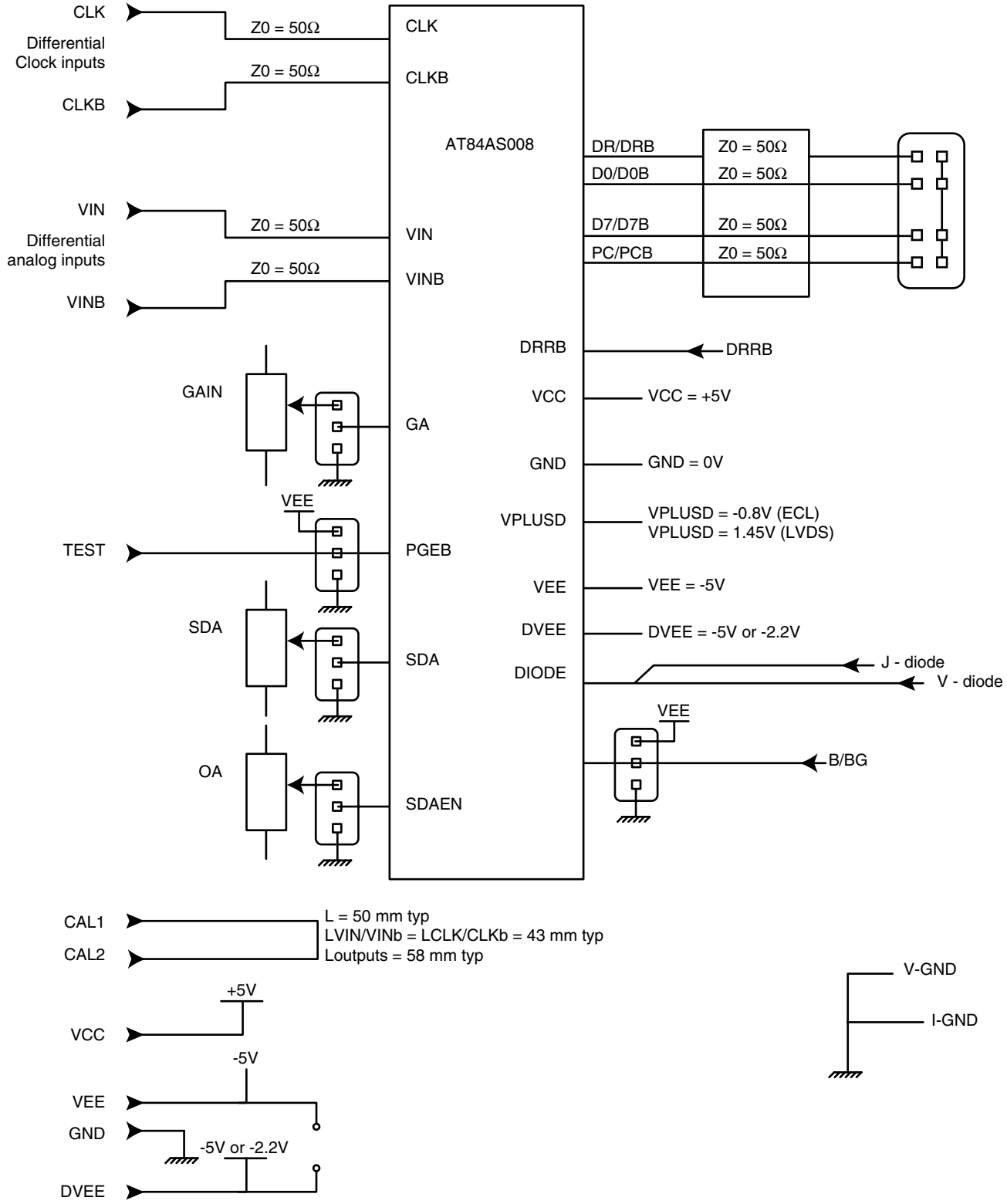
The board also implements a de-embedding fixture in order to facilitate the evaluation of the high frequency insertion loss of the input microstrip lines. It comprises two dielectric layers, featuring low insertion loss and enhanced thermal characteristics for operation in the high frequency domain and extended temperature range.

The board's dimensions are 120 mm × 150 mm.

The board set comes fully assembled and tested, with the AT84AS008 installed and features a heatsink.

1.2 AT84AS008-EB Evaluation Board

Figure 1-1. AT84AS008-EB Block Diagram



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1.3 Board Mechanical Characteristics

The board's layer number, thickness and functions are given in Table 1-1, from top to bottom.

Table 1-1. Board's Layer Thickness Profile

Layer	Characteristics
Layer 1 Copper layer	Thickness of copper = 40 µm AC signal traces = 50Ω microstrip lines DC signal traces (B/GB, GAIN, DIODE, OA, TEST, SDA)
Layer 2 RO4003 dielectric layer (Hydrocarbon/Wovenglass)	Thickness of layer = 200 µm Dielectric constant = 3.4 at 10 GHz -0.044 dB/inch insertion loss at 2.5 GHz -0.318 dB/inch insertion loss at 18 GHz
Layer 3 Copper layer	Thickness of copper = 39 µm Ground plane = reference plane 50Ω microstrip return
Layer 4 BT/Epoxy dielectric layer	Thickness of layer = 330 µm
Layer 5 Copper layer	Thickness of copper = 35 µm Power and ground planes
Layer 6 BT/Epoxy dielectric layer	Thickness of layer = 330 µm
Layer 7 Copper layer	Thickness of copper = 35 µm Power and ground planes (identical to layer 5)
Layer 8 BT/Epoxy dielectric layer	Thickness of layer = 330 µm
Layer 9 Copper layer	Thickness of copper = 35 µm Ground planes (identical to layer 3)
Layer 10 BT/Epoxy dielectric layer	Thickness of layer = 200 µm
Layer 11 Copper layer	Thickness of copper = 35 µm Power and ground planes

The AT84AS008-EB is an eleven-layer PCB made of six copper layers and five dielectric layers. The six metal layers correspond respectively from top to bottom to the AC and DC signals' layer (layer 1), two ground layers (layers 3 and 5), and one supply layer (layer 7).

Considering the severe mechanical constraints due to the wide temperature range and the high frequency domain in which the board is to operate, it is necessary to use a "sandwich" of two different dielectric materials, with specific characteristics:

- A low insertion loss RO4003 Hydrocarbon/Wovenglass dielectric layer 200 µm thick, chosen for its low loss (-0.318 dB/inch) and enhanced dielectric consistency in the high frequency domain. The RO4003 dielectric layer is dedicated to the routing of the 50Ω impedance signal traces (the RO4003 typical dielectric constant is 3.4 at 10 GHz). The RO4003 dielectric layer characteristics are very close to PTFE in terms of insertion loss characteristics
- A BT/Epoxy dielectric layer 0.99 mm thick (total) sandwiched between the upper ground plane and the back-side supply layer

The BT/Epoxy layer has been chosen because of its enhanced mechanical characteristics for elevated temperature operation. The typical dielectric constant is 4.5 at 1 MHz.

More specifically, the BT/Epoxy dielectric layer offers enhanced characteristics compared to FR4 Epoxy, namely:

- Higher operating temperature values: 170°C (125°C for FR4)
- Higher resistance to thermal shocks (-65°C up to 170°C)

The total thickness of the board is 1.6 mm. The previously-described mechanical and frequency characteristics make the board particularly suitable for device evaluation and characterization in the high frequency domain and in military temperature ranges.

1.4 Analog Input, Clock Input and De-embedding Fixture Accesses

The differential active inputs (analog, clock, de-embedding fixture) are provided by SMA connectors.

Reference: VITELEC 142-0701-851.

Connector mounting plates have been used to fasten the SMA connectors.

1.5 Digital Outputs Accesses

Access to the differential output data port is provided by a 2.54 mm pitch connector, compatible with the high-speed digital acquisition system. It provides access to the converter output data, as well as proper 50Ω differential termination.

1.6 Power Supplies and Ground Accesses

The power supply accesses are provided by five 2 mm section banana jacks respectively for DV_{EE}, V_{PLUSD} and V_{CC}.

The power supply access is provided by one 4 mm section banana jack for V_{EE}.

The ground accesses are provided by four 2 mm and one 4 mm banana jacks.

1.7 ADC Function Setting Accesses

For ADC function setting accesses (B/GB, die junction temp., test), 2 mm section banana jacks are provided.

Three potentiometers are provided for ADC gain, sampling delay and offset adjustments.

One sub-screw is provided for asynchronous data ready reset.

Note: OA refers to SDAEN
Test refers to PGEB
PC/PCb refers to OR/ORb

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Section 2
Layout Information

2.1 Board

The AT84AS008 requires appropriate board layout for optimum full-speed operation.

The following explains the board layout recommendations and demonstrates how the Evaluation Board fulfills these implementation constraints.

A single low impedance ground plane is recommended, since it allows the user to lay out signal traces and power planes without interrupting the ground plane.

A multi-layer board structure has therefore been retained for the AT84AS008-EB.

Six copper metal layers are used, dedicated to the signal traces, ground planes and power supplies respectively (from top to bottom).

2.2 AC Inputs/Digital Outputs

The board uses 50Ω impedance microstrip lines for the differential analog inputs, clock inputs, and differential digital outputs.

The input signals and clock signals must be routed on one layer only, without use of any through-hole vias. The line lengths are matched to within 2 mm.

The digital output lines are 50Ω differentially terminated.

The output data trace lengths are matched to ± 1 mm to minimize the data output delay skew.

For the AT84AS008-EB the propagation delay is approximately 6.1 ps/mm (155 ps/inch). The RO4003 typical dielectric constant is 3.4 at 10 GHz.

For more information about different output termination options refer to the specification application note entitled “Input/Output Termination Techniques” (reference 2169).

2.3 DC Function Settings

The DC signal traces are low impedance.

They have been routed with a 50Ω impedance near the device because of space restriction.

2.4 Power Supplies

The bottom metal layers 5, 7 and 11 are dedicated to power supply traces (V_{EE}, DV_{EE}, V_{PLUSD} and V_{CC}).

The supply traces are approximately 6 mm wide in order to present low impedance, and are surrounded by a ground plane connected to the two inner ground planes.

No difference in ADC high-speed performance has been observed when connecting both negative supply planes together. Obviously one single negative supply plane could be used for the circuit.

Each incoming power supply is bypassed by a 1 µF Tantalum capacitor in parallel with 1 nF chip capacitor.

Each power supply access is decoupled very close to the device by 10 nF and 100 pF surface-mount chip capacitors in parallel.

Note: The decoupling capacitors are superposed. In this configuration, the 100 pF capacitors must be mounted first.

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Section 3

Operating Procedures and Characteristics

3.1 Introduction

This section describes a typical single-ended configuration for the analog and clock inputs.

The single-ended configuration is preferable, as it corresponds to the most straightforward and quickest AT84AS008-EB board setting for evaluating the AT84AS008 at full speed in its given temperature range.

The inverted analog input V_{INB} and clock input CLKB common mode level is ground (on-chip 50Ω-terminated). In this configuration, no balun transformer is needed to correctly convert the single-ended mixer output to balanced differential signals for the analog inputs.

In the same way, no balun is necessary to feed the AT84AS008 clock inputs with balanced signals.

The RF sources should be directly connected to the in-phase analog and clock inputs of the converter. However, dynamic performances can be somewhat improved by entering either analog or clock inputs in differential mode.

3.2 Operating Procedure (ECL Mode)

1. Connect the power supplies and ground accesses
(V_{CC} = +5V, GND = 0V, V_{PLUSD} = 0V, V_{EE} = -5V, DV_{EE} = -5V or -2.2V) through the dedicated banana jacks.
We recommend you turn the -5V power supply on first (followed by -2.2V if applicable, followed by 5V).

2. The board is set to default digital outputs in binary format.

3. Connect the CLK clock signal. The inverted phase clock input CLKB may be 50Ω terminated. Use a low phase noise RF source. The clock input level is typically 4 dBm and should not exceed +10 dBm into the 50Ω termination resistor (maximum ratings for the clock input power level is 15 dBm).

4. Connect the analog signal V_{IN}. The inverted phase clock input V_{INB} may be 50Ω terminated. Use a low phase noise RF source. The full-scale range is 0.5V peak-to-peak around 0V (±250 mV) or -2 dBm into 50Ω.
The input frequency can range from DC up to 1.8 GHz. At 3.3 GHz, the ADC attenuates the input signal by -3 dB.

5. Connect the high-speed data acquisition system probes to the output connector. The connector pitch (2.54 mm) is compatible with high-speed digital acquisition system probes. The digital data is on-board differentially terminated. However, the output data can be picked up either in single-ended or differential mode.

3.3 Use with DMUX Evaluation Board

The AT84CS001-EB DMUX evaluation board has been designed for full compatibility with the AT84AS008-EB ADC evaluation board.

The DEMUX input configuration has been optimized for connection with the AT84AS008 ADC (CBGA152 package).

For correct operation, when using the DMUX board with the ADC board, do not forget to set CLKINTYPE to DR/2 mode (jumper on-board).

The power-up sequence should be:

1. Supply the ADC
2. Supply the DMUX
3. Perform an asynchronous reset on the DMUX board

When this power-up sequence has been completed, synchronization between the DMUX and ADC boards can be achieved via the CLKDACTRL potentiometers on the DMUX evaluation board. To correctly synchronize the two boards, we recommend that you run the ADC at its full-speed (maximum sampling rate) and tune the DMUX Delay Adjust Control potentiometer to the left, noting the settings at which the boards are de-synchronized, and similarly tune the potentiometer to the right to identify the point of loss of synchronization at the other extremity. The correct potentiometer setting should be half-way between these two settings and should be accurate for all sampling rates of the ADC.

When used with the AT84CS001, then there are two solutions:

- V_{PLUSD} = 1.45V and DV_{EE} = -5V (or -2.2V, for power saving)
- V_{PLUSD} = 2.5V and DV_{EE} = -2.2V

3.4 Electrical Characteristics

Table 3-1. Absolute Maximum Ratings

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V_{CC}		GND to 6.0	V
Digital negative supply voltage	DV_{EE}		GND to -5.5 or -2.2V	V
Digital positive supply voltage	V_{PLUSD}		GND -1.1 to 2.5	V
Negative supply voltage	V_{EE}		GND to -5.5	V
Maximum difference between negative supply voltages	DV_{EE} to V_{EE}		0.3	V
Maximum difference between V_{PLUSD} and D_{VEE}	V_{PLUSD} - D_{VEE}		7	V
Analog input voltages	V_{IN} or V_{INB}		-1.5 to +1.5	V
Maximum difference between V_{IN} and V_{INB}	V_{IN} - V_{INB}		-1.5 to +1.5	V
Clock input common mode voltage	$(V_{CLK} + V_{CLKB})/2$		-1.5 to +0.6	V
Maximum difference between V_{CLK} and V_{CLKB}	V_{CLK} - V_{CLKB}		-1 to +1	V
Static input voltage	V_D	GA/SDA	-1 to +0.8	V
Digital input voltage	V_D	SDAEN, DRRB, B/GB, PGEB	-5 to +0.8	V
Digital output voltage	V_O		V_{PLUSD} -2.2 to V_{PLUSD} +0.8	V
Maximum junction temperature	T_j		+130	°C
Storage temperature	T_{stg}		-65 to +150	°C
Lead temperature (soldering 10s)	T_{leads}		+300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability. The use of a thermal heat sink is mandatory.

3.5 Operating Characteristics

The power supplies denoted by V_{CC}, V_{EE}, DV_{EE} and V_{PLUSD} are dedicated to the AT84AS008 ADC.

The power supplies denoted by V_{EET}, V_{DD} are dedicated to the optional MC100EL16 asynchronous differential receivers.

Table 3-2. Electrical Operating Characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Positive supply voltage (dedicated to AT84AS008 ADC only)	V_{CC}	4.75	5	5.25	V
	V_{PLUSD}	-0.9 1.375	ECL: -0.8 LVDS: 1.45 2.5(1)	-0.7 1.525	V
	V_{EEA}	-5.25	-5	-4.75	V
	DV_{EE}	-5.25 -2.3	-5 -2.2(2)	-4.75 -2.1	V
Positive supply current (dedicated to AT84AS008 ADC only)	I_{CC}	–	75	100	mA
	I_{PLUSD}	–	195	230	mA
	I_{EE}	–	590	660	mA
	I_{EED}	–	195	230	mA
Nominal power dissipation (ECL)	PD	–	4.2	4.7 (T_J = 125°C)	W
Analog input impedance	Z_{IN}	–	50	–	Ω
Full power analog input bandwidth (-3 dB)	–	–	3.3	–	GHz
Analog input voltage range (differential mode)	V_{IN}	-125	–	125	mV
Clock input impedance	–	–	50	–	Ω
Clock input voltage compatibility (single-ended or differential) (See Application Notes)	–	ECL levels or 0 dBm (typ) into 50Ω			–
Clock input power level into 50Ω termination resistor	–	-4	0	4	dBm

Note: 1. If the ADC is used with the AT84CS001-EB DMUX evaluation board, V_{PLUSD} can be set to 2.5V so that the same supply can be used for V_{PLUSD} (ADC) and V_{PLUSD} (DMUX). In this case, DV_{EE} must be set to -2.2V.

2. To save power, DV_{EE} can be set to -2.2V. In this case, V_{PLUSD} must be either 1.5V or 2.5V.

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Section 4
Application Information

4.1 Introduction

For this section, also refer to the product's "Main Features" in the datasheet of the AT84AS008 device (reference 5404A). More particularly, refer to sections related to single-ended and differential input configurations.

4.2 Analog Inputs

The analog inputs can be entered in differential or single-ended mode without degrading the high-speed performance of the device.

The board digitizes single-ended signals by selecting either input and leaving the other input open, as the latter is on-board 50Ω terminated. The nominal in-phase inputs are V_{IN} (refer to Section 3).

4.3 Clock Inputs

The clock inputs can be entered in differential or single-ended mode without degrading performance of the device for a clock frequency up to 500 MHz. At higher rates, we recommend that you drive the clock inputs differentially. Moreover, the typical in-phase clock input amplitude is 1V peak-to-peak, centered on 0V (ground), or -1.3V (ECL) in common mode.

Regarding the analog input, either clock input can be chosen (if the single-ended output mode is used), leaving the other input open, as both clock inputs are on-chip 50Ω terminated. The nominal in-phase clock input is CLK (refer to Section 3).

4.4 Setting the Digital Output Data Format

For this section, refer to the Evaluation Board Electrical schematic and to the components placement document (respectively Figure 6-2 on page 6-3 and Figure 6-8 on page 6-5).

Please also refer to the AT84AS008 datasheet (reference 5404A) for more information on digital output coding.

The AT84AS008 delivers data in natural binary code or in Gray code. If the B/GB input is left floating or tied to GND, the data format selected will be natural binary, whereas if this input is tied to V_{EE} the data will follow the Gray code.

Use the jumper designated B/GB to select the output data port format:

- If B/GB is left floating or tied to GND, the data output format is true binary
- If B/GB is tied to V_{EE} or driven with ECL low, the data outputs are in the Gray format

The V_{PLUSD} positive supply voltage is used to adjust the output common mode level from -1.05V (V_{PLUSD} = -0.8V for ECL output compatibility) to +1.35V (V_{PLUSD} = 1.45V for LVDS output compatibility).

Each output voltage varies between -0.9V and -1.2V (respectively +1.2V and +1.5V), leading to ±0.3V = 660 mV in differential mode for V_{PLUSD} = -0.8V (respectively 1.45V).

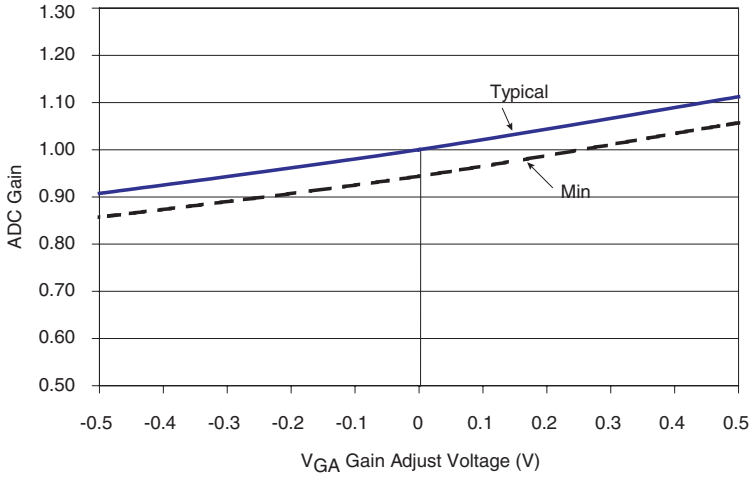
4.5 ADC Gain Adjust

The ADC gain can be adjusted through pin R9 (pad input impedance is 1 MΩ in parallel with 2 pF). A jumper denoted GAIN has been foreseen in order to provide access to the ADC gain adjust pin.

The GAIN potentiometer is dedicated to adjusting the ADC gain from approximately 0.85 up to 1.15.

The gain adjust transfer function is given below.

Figure 4-1. ADC Gain Adjust



4.6 SMA Connectors and Microstrip Lines De-embedding Fixture

Attenuation in microstrip lines can be found by calculating the difference in the log magnitudes of the S21 scattering parameters measured on two different lengths of meandering transmission lines.

Such a measurement also removes common losses such as those due to transitions and connectors.

The S21 scattering parameter corresponds to the amount of power transmitted through a two-port network.

The characteristic impedance of the microstrip meander lines must be close to 50Ω to minimize impedance mismatching with the 50Ω network analyzer test ports.

Impedance mismatching will cause ripples in the S21 parameter according to the degree of mismatch and the length of the line.

4.7 Die Junction Temperature Monitoring

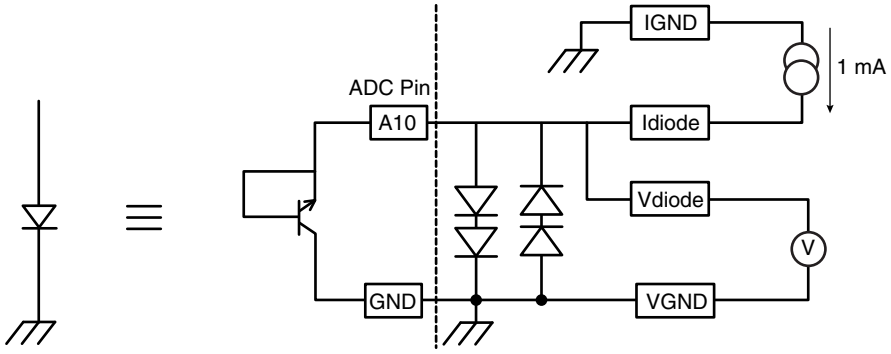
Figure 4-2 and Figure 4-3 show the recommended implementation of the die junction temperature monitoring function.

There are two possible configurations:

1. The ADC decimation test mode is not authorized.

Due to the use of one internal diode-mounted transistor, you must implement 2 × 2 head-to-tail protection diodes to avoid potential reverse current flows that may damage the diode pin.
Note that e2v usually recommends the use of 2 × 3 head-to-tail protection diodes but in this particular case, it is necessary to have exactly two diodes in the A10 to ground conduction flow.

Figure 4-2. Recommended Die Junction Temperature Monitoring Function Implementation, Test Mode not Allowed



2. The ADC decimation test mode is authorized

If you still want to be able to switch from normal mode to test mode or to the die junction temperature monitoring function, the protection diode configuration will be slightly different and will take into account the fact that the test mode can be activated by applying V_{EE} = -5V to the diode pin.
This explains why seven protection diodes are needed in the reverse direction, as described in Figure 4-3.

Figure 4-3. Recommended Diode Pin Implementation Providing for Both Die Junction Temperature Monitoring Function and Test Mode

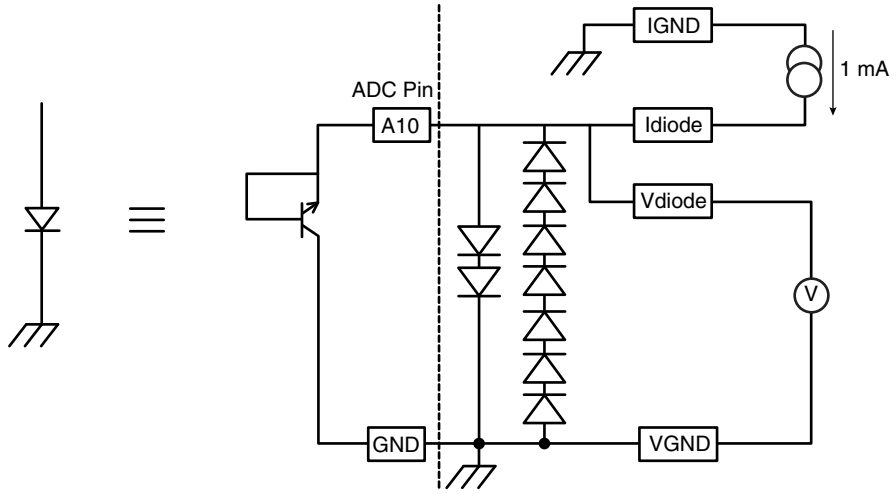
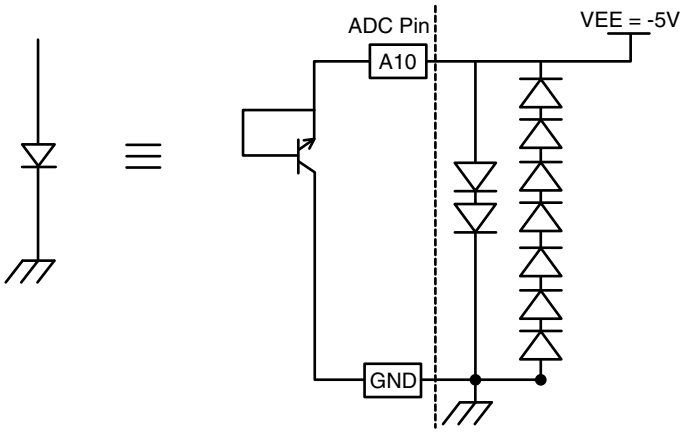
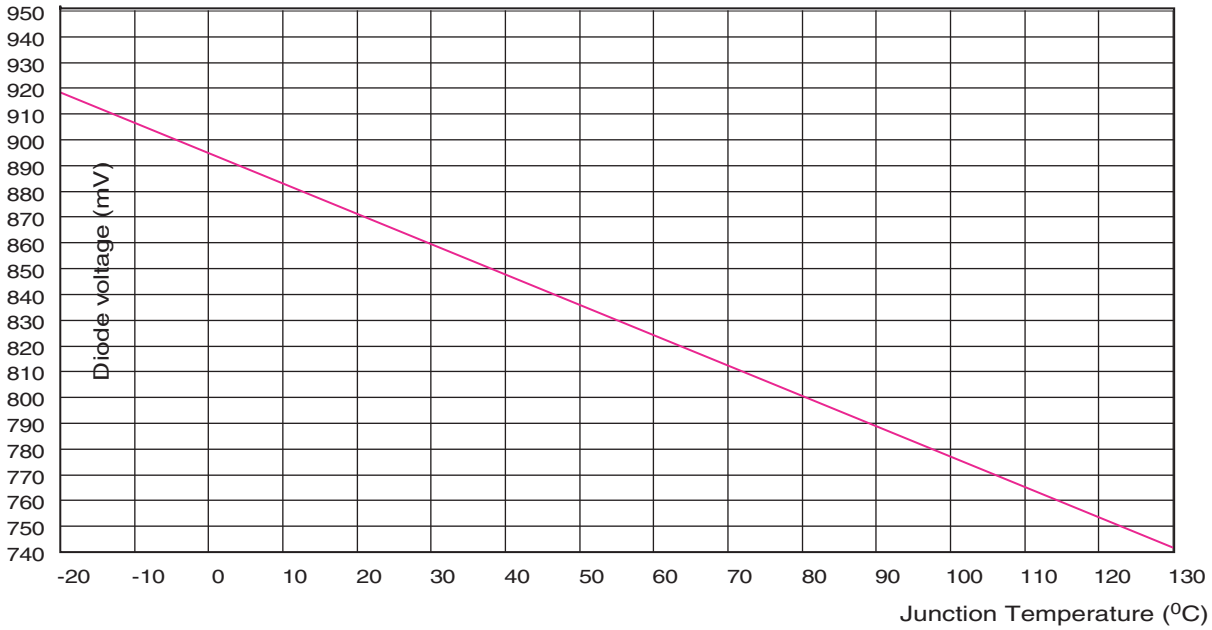


Figure 4-4. Diode Pin Implementation in Test Mode



The expected diode-mounted transistors V_{DIODE} value (including chip parasitic resistance) compared to the junction temperature is given in Figure 4-5 (I_{DIODE} = 1 mA).

Figure 4-5. Junction Temperature Versus Diode Voltage for I = 1 mA



Note: The operating die junction temperature must be kept below 125°C; this requires that an adequate cooling system be set up.

4.8 Decimation Function

The decimation function can be used for initial stage debugging of the ADC. This function enables reduction of the ADC output rate by 32, thus allowing for a quick debug phase of the ADC at maximum speed rate.

When active, this function outputs only 1 out of 32 bits of data, thus resulting in a data rate 32 times slower than the clock rate.

4.9 Pattern Generator Enable

The AT84AS008 is able to self-generate (with no analog input signal) a series of patterns. If the TEST input is left floating or tied to GND, the AT84AS008 digitizes the analog input signal according to B/GB. If this input is driven with ECL low or tied to V_{EE}, the AT84AS008 generates checker-board patterns.

Use the jumper named TEST to activate the pattern generator.

4.10 Data Ready Output Signal Reset

A sub-screw connector is provided for the DRRB command.

The Data Ready signal is reset on the falling edge of the DRRB input command, on ECL logical low level (-1.8V). DRRB may also be tied to V_{EE} = -5V for Data Ready output signal master reset. As long as DRRB remains at a logical low level, (or tied to V_{EE} = -5V), the Data Ready output remains at logical zero and is independent of the external free running encoding clock.
The Data Ready output signal (DR, DRB) is reset to logical zero after TRDR = 720 ps typically.

TRDR is measured between the -1.3V point of the falling edge of the DRRB input command and the zero crossing point of the differential Data Ready output signal (DR, DRB).

The Data Ready Reset command may be a pulse of 1 ns minimum time width.
The Data Ready output signal restarts on the DRRB command's rising edge, ECL logical high level (-0.8V).

DRRB may also be grounded, or left floating, for normal free running of the Data Ready output signal.

4.11 Sampling Delay Adjusting

One delay adjust, controlled by the SDA potentiometer, is available in order to add a delay to the ADC's input clock. This allows you to tune the instant of internal sampling. To enable this delay adjustment there is an SDAEN pin on the chip. In the current revision, the SDAEN function corresponds to the OA labels (OA jumper and OA potentiometer).

The OA potentiometer has been removed and short-circuited to V_{EE}.

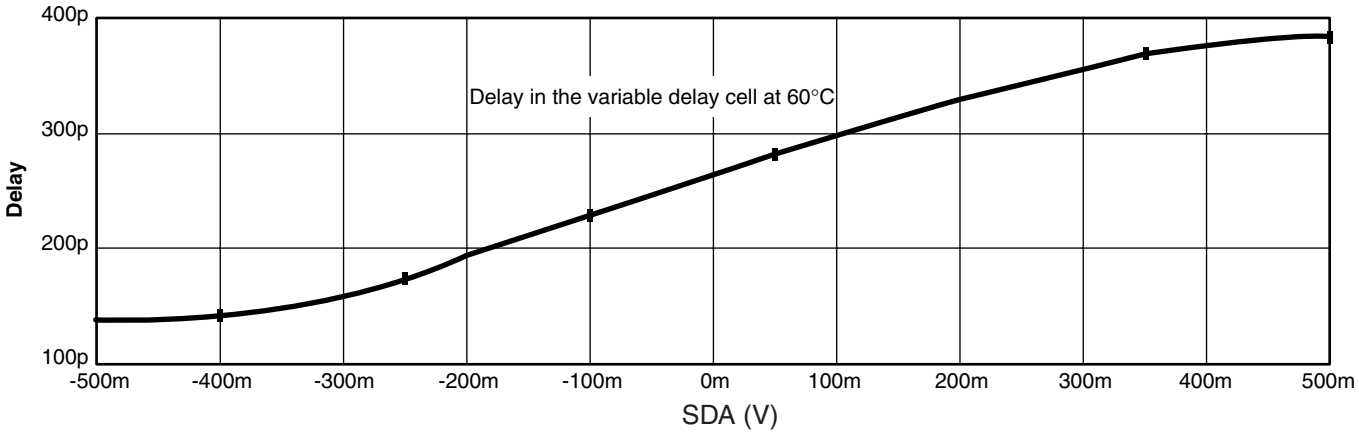
Use the jumper named OA to activate the sampling delay adjustment:

- If OA is left floating or tied to GND, the SDA is disabled
- If OA is tied to V_{EE}, the SDA is activated

The SDA input varies from -0.5 to 0.5V, depending on the SDA's potentiometer position.

The delay variation around its nominal value according to the SDA voltage is more or less linear, as shown in Figure 4-6 (simulation results).

Figure 4-6. Sampling Delay Adjust



Note: The delay variation according to temperature is insignificant.

4.12 Test Bench Description

Figure 4-7. Differential Analog and Clock Input Configuration

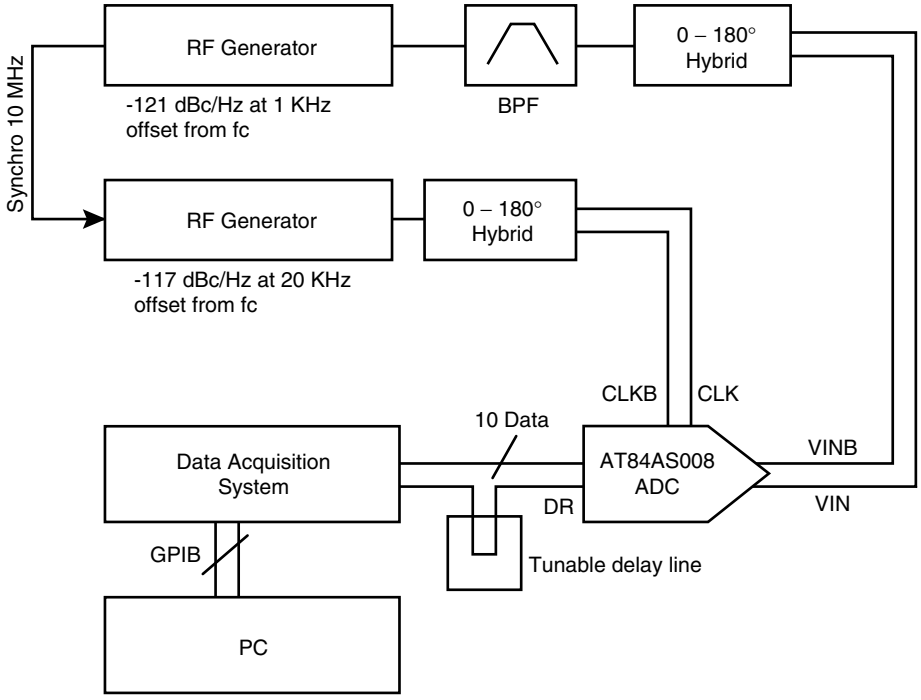
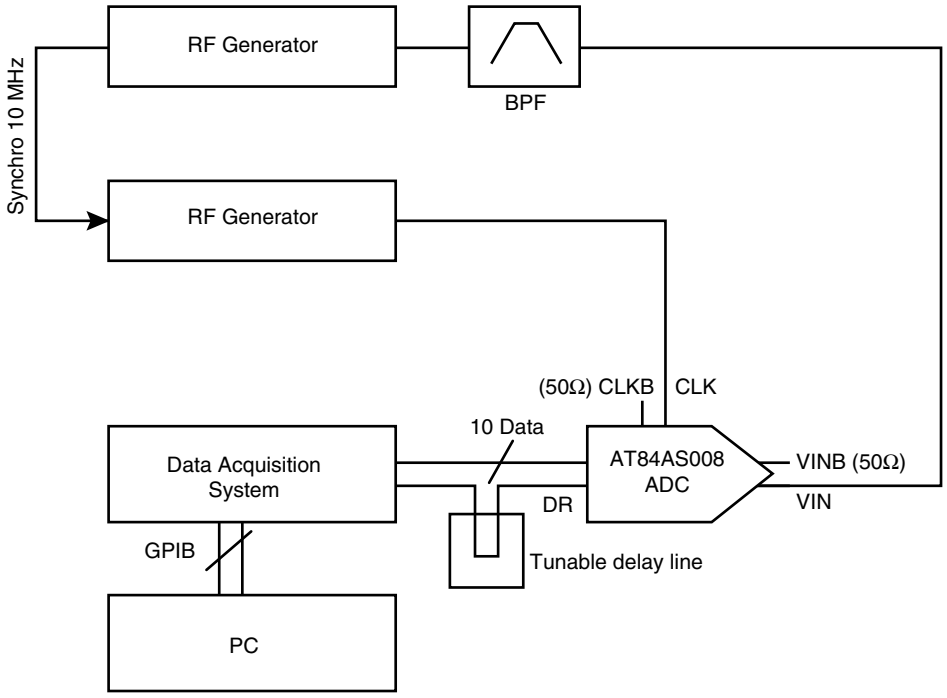


Figure 4-8. Single-ended Analog and Clock Input Configuration

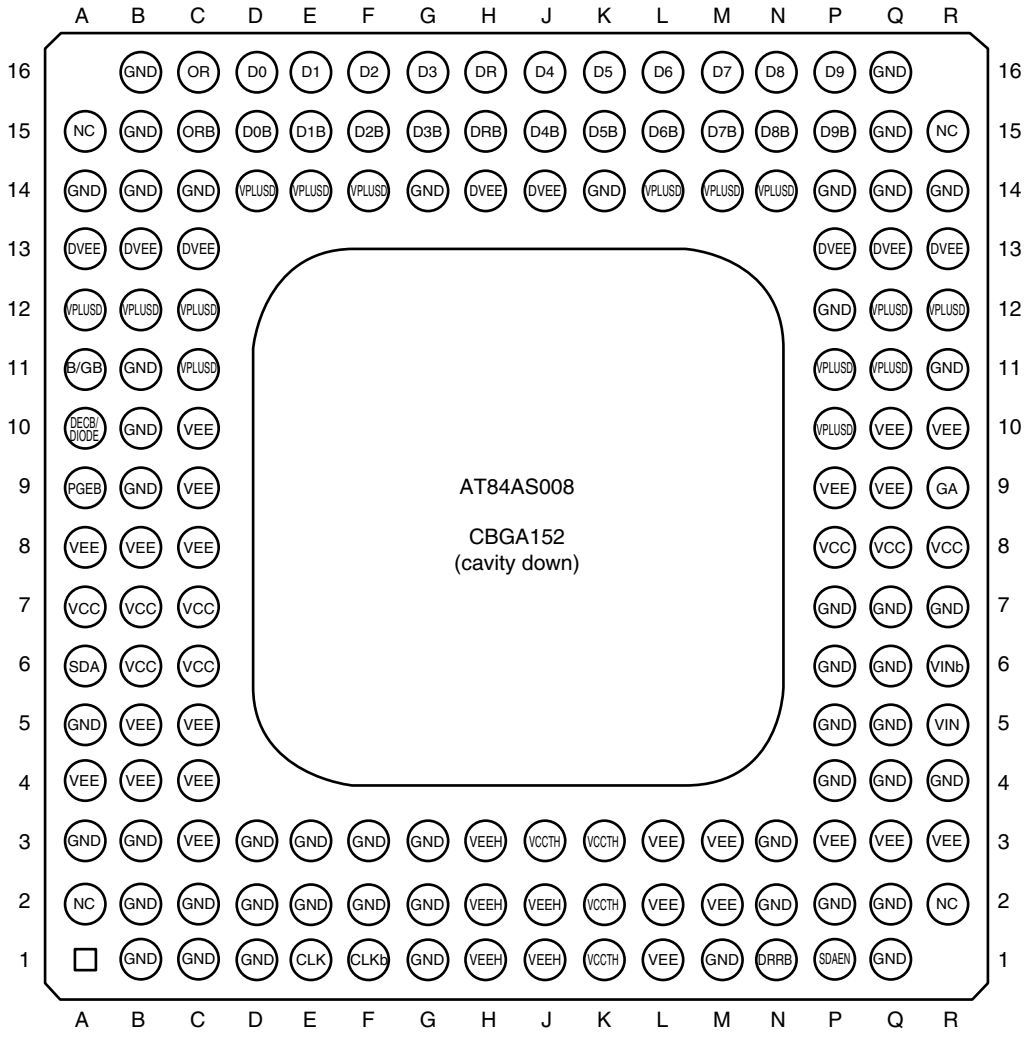


Section 5

Package Description

5.1 AT84AS008 Pinout

Figure 5-1. AT84AS008 Pinout of CBGA152 Package (Bottom View)



Note: If required, four NC balls can be electrically connected to GND to simplify PCB routing.

Table 5-1. AT84AS008-EB Pin Description

Symbol	Pin Number	Function
Power Supplies		
V_{CC}	K1, K2, J3, K3, B6, C6, A7, B7, C7, P8, Q8, R8	+5V analog supply
GND	B1, C1, D1, G1, M1, Q1, B2, C2, D2, E2, F2, G2, N2, P2, Q2, A3, B3, D3, E3, F3, G3, N3, P4, Q4, R4, A5, P5, Q5, P6, Q6, P7, Q7, R7, B9, B10, B11, R11, P12, A14, B14, C14, G14, K14, P14, Q14, R14, B15, Q15, B16, Q16	Analog ground
V_{EE}	H1, J1, L1, H2, J2, L2, M2, C3, H3, L3, M3, P3, Q3, R3, A4, B4, C4, B5, C5, A8, B8, C8, C9, P9, Q9, C10, Q10, R10	-5V analog supply
V_{PLUSD}	P10, C11, P11, Q11, A12, B12, C12, Q12, R12, D14, E14, F14, L14, M14, N14	Digital positive supply
DV_{EE}	A13, B13, C13, P13, Q13, R13, H14, J14	-5V or -2.2V digital supply
Analog Inputs		
V_{IN}	R5	In-phase (+) analog input signal of the differential sample and hold preamplifier
V_{INB}	R6	Inverted phase (-) analog input signal of the differential sample and hold preamplifier
Clock Inputs		
CLK	E1	In-phase (+) clock input
CLKB	F1	Inverted phase (-) clock input
Digital outputs		
D0, D1, D2, D3, D4, D5, D6, D7, D8, D9	D16, E16, F16, G16, J16, K16, L16, M16, N16, P16	In-phase (+) digital outputs D0 is the LSB. D9 is the MSB
D0B, D1B, D2B, D3B, D4B, D5B, D6B, D7B, D8B, D9B	D15, E15, F15, G15, J15, K15, L15, M15, N15, P15	Inverted phase (-) digital outputs
OR	C16	In-phase (+) Out-of-Range output
ORB	C15	Inverted phase (-) Out-of-Range output
DR	H16	In-phase (+) Data Ready Signal output
DRB	H15	Inverted phase (-) Data Ready Signal output
Additional Functions		
B/GB	A11	Binary or Gray select output format control - Binary output format if B/GB is floating or connected to GND - Gray output format if B/GB is driven with ECL low level or B/GB is connected to V_{EE}

Table 5-1. AT84AS008-EB Pin Description (Continued)

Symbol	Pin Number	Function
DIODE	A10	Decimation function enable or die junction temperature monitoring: - Decimation active when LOW (die junction temperature monitoring NOT possible) - Normal mode when HIGH or left floating - Die junction temperature monitoring when current is applied
PGEB	A9	Active low pattern generator enable - Digitized input delivered at outputs according to B/GB if PGEB is floating or connected to GND - Checkerboard pattern delivered at outputs if PGEB is driven with ECL low level or connected to V_{EE}
DRRB	N1	Asynchronous Data Ready Reset function
GA	R9	Gain Adjust
SDA	A6	Sampling delay adjust
SDAEN	P1	Sampling delay adjust enable: - inactive if floating or connected to GND - active if ECL low or connected to V_{EE}

5.2 Thermal Characteristics

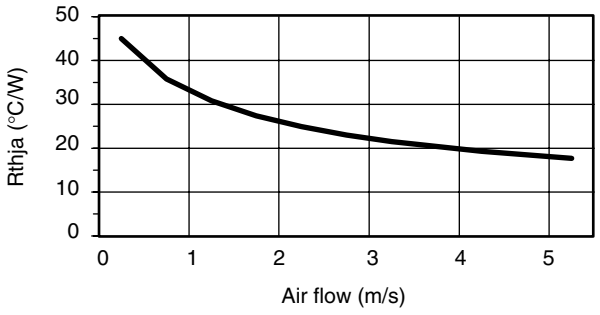
5.2.1 Thermal Resistance from Junction to Ambient: Rthja

Table 5-2 lists the converter's thermal performance parameters with no external heat sink added.

Table 5-2. Thermal Resistance

Air Flow (m/s)	Estimated ja Thermal Resistance (°C/W)
0	45
0.5	35.8
1	30.8
1.5	27.4
2	24.9
2.5	23
3	21.5
4	19.3
5	17.7

Figure 5-2. Thermal Resistance from Junction to Ambient: Rthja



5.2.2 Thermal Resistance from Junction to Case: Rthjc

The maximum thermal junction-to-case resistance is 4.0°C/watt.

This value does not include thermal contact resistance between the package and external heat sink (glue, paste or thermal foil interface for example).

As an example, we will use 2.0°C/W for a 50 µm thickness of thermal grease.

5.2.3 Heat Sink

We recommend that you use a 50 × 50 × 30 mm heat sink (respectively L × l × H) when in natural convection-cooling mode (with no air flow).

A fan heat sink or direct conduction cooling is recommended, due to high power dissipation (4.7W).

A cooling method should be chosen that permits less than 4.0°C/W for the case-to-ambient thermal resistance (Rthca).

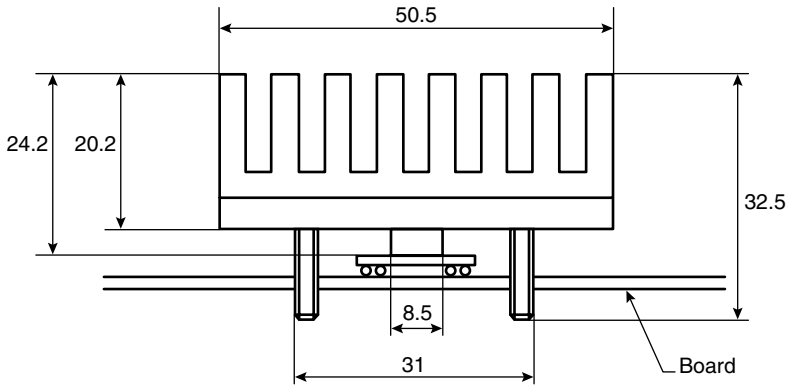
The thermal resistance of the board is a high value (within a range of 30°C/W); thus an external heat sink is mandatory.

The heat sink must be fixed to the heat spreader which is at -5V. The heat sink must therefore be electrically isolated using adequate low Rth electrical isolation.

Example: 4.0°C/W Rthca (case-to-ambient) + 2.0°C/W thermal grease resistance + 4.0°C/W Rthjc = 10.0°C/W total (Rthja).

The heat sink should be in contact with the package on the side opposite to the balls, in a 8.5 mm diameter circle as shown in Figure 5-3:

Figure 5-3. CBGA152 Board Assembly



Note: The measures are given in mm.

The efficiency of the cooling system can be monitored using the temperature sensing diodes integrated in the device.

5.3 Ordering Information

Table 5-3. Ordering Information

Part Number	Package	Temperature Range	Screening Level	Comments
AT84XAS008GL	CBGA 152	Ambient	Prototype	Prototype version
AT84AS008CGL	CBGA 152	“C” grade: 0°C <T_C; T_J <90°C	Standard	
AT84AS008VGL	CBGA 152	“V” grade: -20°C <T_C; T_J <110°C	Standard	
AT84AS008CGLY	CBGA 152 RoHS	Commercial "C" grade 0°C < T_C; T_J < 90°C	Standard	
AT84AS008VGLY	CBGA 152 RoHS	Industrial "V" grade -20°C < T_C; T_J < 110°C	Standard	
AT84AS008GL-EB	CBGA 152	Ambient	Prototype	Evaluation board (delivered with heat sink)

Section 6

Schematics

6.1 AT84AS008-EB Electrical Schematic

Figure 6-2 to 6-8 depict the electrical schematic of the AT84AS008-EB.

The pinout used for the evaluation board has been translated from e2v's pinout (refer to “AT84AS008 Pinout of CBGA152 Package (Bottom View)” on page 5-1) to the JEDEC standard shown in Figure 6-1. This explains the discrepancies between the pinout used on page 5-1 and the one given in the electrical schematic in Figures 6-2 on page 6-2.

Figure 6-1. AT84AS008 pinout in JEDEC Standard

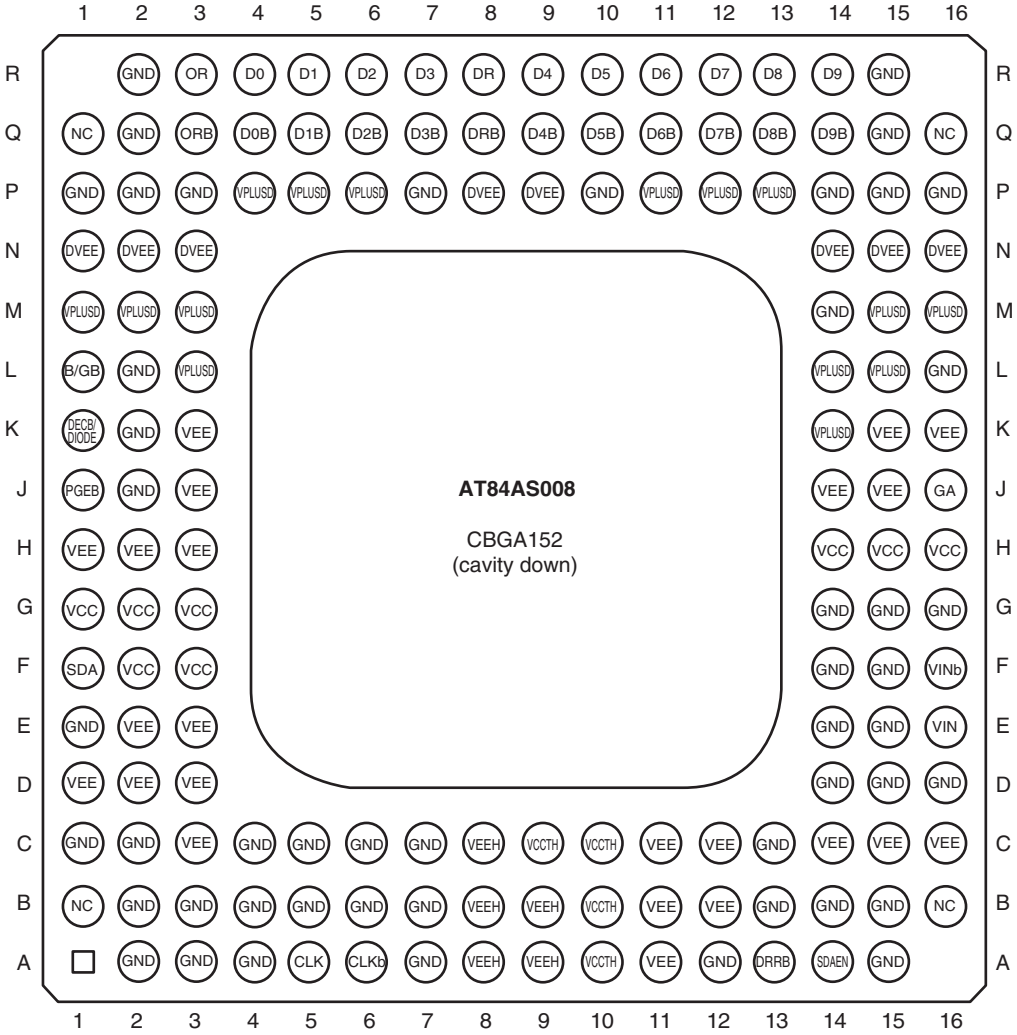


Figure 6-2. AT84AS008-EB Electrical Schematic

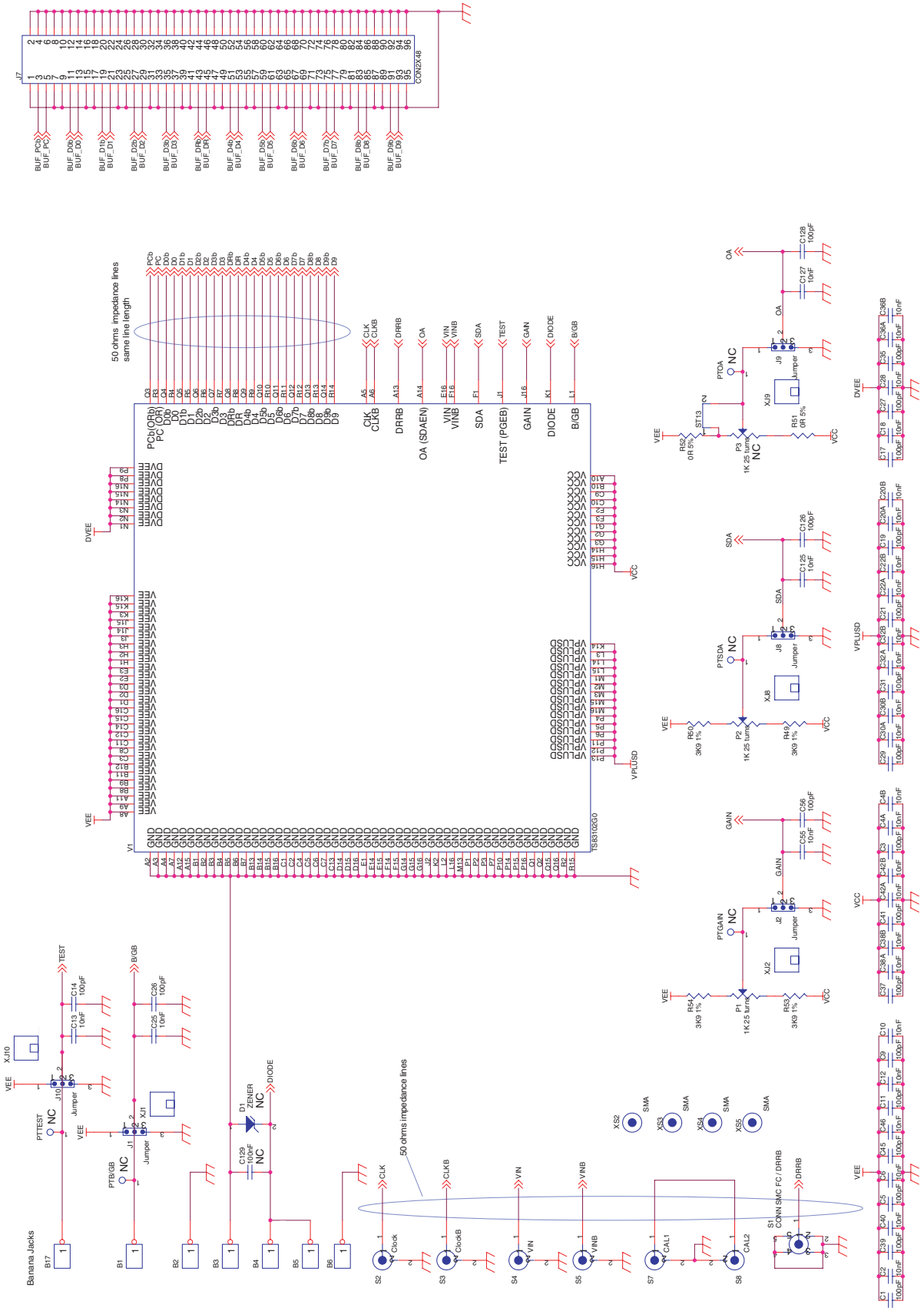


Figure 6-3. Component Side Description

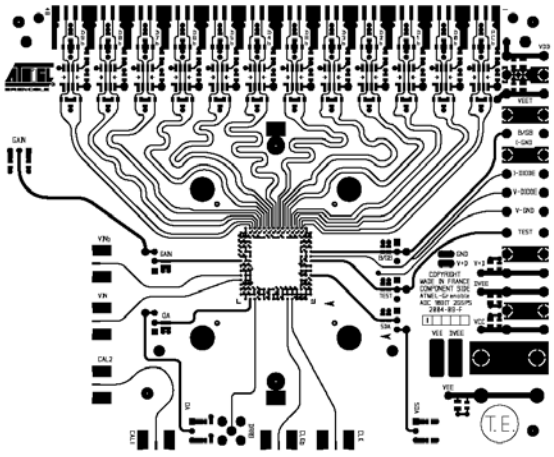


Figure 6-4. Metal Layer 2 and 4: Ground Planes

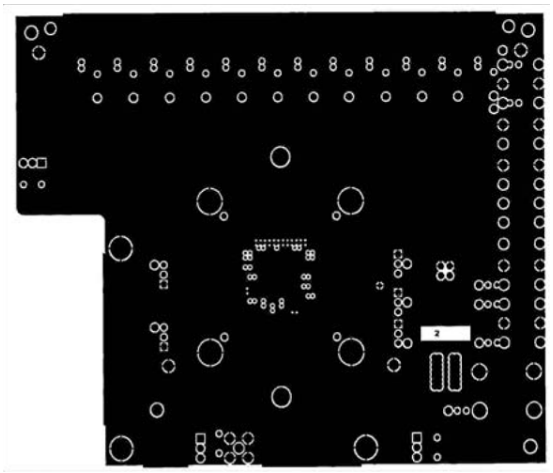


Figure 6-5. Metal Layer 3 and 3 bis: Power Supplies and Ground Planes

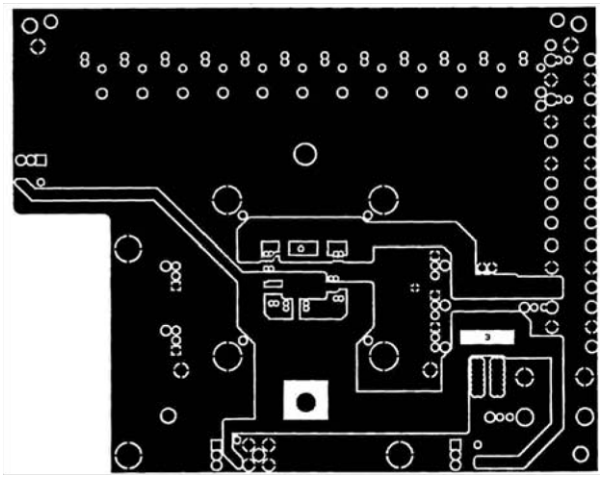


Figure 6-6. Metal Layer 5: Solder Side

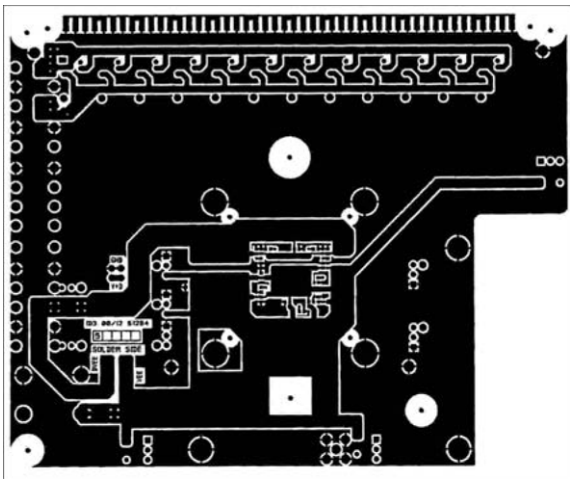


Figure 6-7. AT84AS008-EB Evaluation Board: Top View (Signal Side) with Heatsink

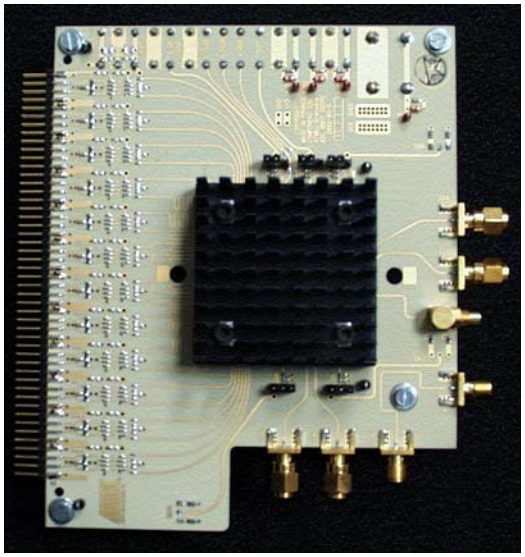
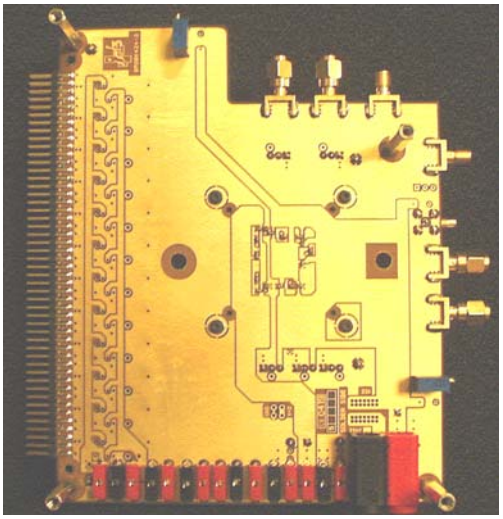


Figure 6-8. AT84AS008-EB Evaluation Board: Bottom View



How to reach us

Home page: www.e2v.com

Sales Office:

Northern Europe

e2v ltd

106 Waterhouse Lane

Chelmsford

Essex CM1 2QU

England

Tel: +44 (0)1245 493493

Fax:: +44 (0)1245 492492

E-Mail: enquiries@e2v.com

Southern Europe

e2v sas

16 Burospace

F-91572 Bièvres

Cedex

France

Tel: +33 (0) 16019 5500

Fax: +33 (0) 16019 5529

E-Mail: enquiries-fr@e2v.com

Germany and Austria

e2v gmbh

Industriestraße 29

82194 Gröbenzell

Germany

Tel: +49 (0) 8142 41057-0

Fax:: +49 (0) 8142 284547

E-Mail: enquiries-de@e2v.com

Americas

e2v inc.

4 Westchester Plaza

Elmsford

NY 10523-1482

USA

Tel: +1 (914) 592 6050 or

1-800-342-5338,

Fax:: +1 (914) 592-5148

E-Mail: enquiries-na@e2v.com

Asia Pacific

e2v

Bank of China Tower

30th floor office 7

1 Garden Rd Central

Hong Kong

Tel: +852 2251 8227/8/9

Fax: +852 2251 8238

E-Mail: enquiries-hk@e2v.com

Product Contact:

e2v

Avenue de Rochepleine

BP 123 - 38521 Saint-Egrève Cedex

France

Tel: +33 (0)4 76 58 30 00

Hotline:

hotline-bdc@e2v.com